

SDG 11.4.3

Allow remote working

Promote or allow telecommuting or remote working for employees as a matter of policy or standard practice, or offer a condensed working week to reduce employee commuting

(1) Telecommuting for M.Tech Degree Classes: As a policy matter to promote remote working, institute allows online classes for four days from Monday to Thursday for M.Tech students. The professors will conduct the online classes from the campus and students attend classes from their residence.

Following subjects were delivered online during M.Tech (VLSI and Embedded system Design) 1st Year I and II Semesters in Academic Year 2021-2022 (Fig. (1) to Fig. (4)).

M.Tech 1st Year I Semester Academic Year 2021-2022 w.e.f 2nd February 2022	
1	16VLS002 Digital Design through VERILOG
2	16VLS102 Embedded System Design
3	19EC002DSP Processors and Architectures
M.Tech 1st Year II Semester Academic Year 2021-2022 w.e.f 4th July 2022	
4	16VLS012 Low Power VLSI Design
5	16VLS013 CPLD and FPGA Architectures & Applications
6	16VLS016 Algorithms for VLSI Design Automation

(2) Telecommuting for Degree with Honours / Minors Classes: The students are allowed to earn 4 credits out of 20 credits for Honours / Minors Degree by taking two 2-Credit MOOCs of 30 hours/6 weeks duration or one 4-Credit MOOCs of 60 hours/12 weeks duration on self-study mode as per the prescribed syllabus.

(3) Telecommuting for B.Tech Degree Classes: The students are allowed to earn the credits of Core Elective, Open Elective and Audit Courses by taking MOOCs on self-study mode as per the prescribed syllabus through NPTEL/COURSERA platforms.

Compiled COURSERA Utilization Report for Year 2022

Phase	Duration		Academic Year	Year/Semester	Learners Enrolled	No. of Courses Completed
	From	to				
Phase-2	10-3-2022	2-7-2022	AY2021-22	3 rd Year/6 th Semester	828	1702
Phase-3	4-7-2022	16-10-2022	AY2022-23	3 rd Year/5 th Semester	1065	4392
	Total				1893	6092

Department : ECE
Year/Semester : Mtech

Academic Year : 2021-2022
Class Room No. : 6-F-01

REV.: 01
6-F-01
w.e.f: 02-02-2022

Timing	Period							
	1	2	3	4	5	6	7	8
Start Time	9:00 AM	9:50 AM	10:50 AM	11:40 AM	1:30 PM	2:20 PM	3:20 PM	4:10 PM
End Time	9:50 AM	10:40 AM	11:40 AM	12:30 PM	2:20 PM	3:10 PM	4:10 PM	5:00 PM
Monday					16VLS102	16DEC002	19EC002	
Tuesday					PK	YM	VK	
Wednesday					19EC002	16VLS102	16DEC002	
Thursday					VK	PK	YM	
Friday			16DEC106		16VLS102	19EC002	16DEC002	
Saturday			Dr J.V Suman		PK	VK	YM	
			16DEC202		16VLS102	16DEC002	19EC002	
			KKK		PK	YM	VK	
					16MEX101	16MEX101	16DEC003	16DEC003
					VSSV	VSSV	DVR	16DEC003
					16DEC003	16DEC003	16MEX101	16MEX101
					DVR	DVR	VSSV	VSSV

Sl. No.	Code	Course Title	Credit	Faculty Name
1	16MEX101	Advanced Optimization Techniques	4	Mr V.S.S. Venkatesh
2	16VLS102	Embedded system design	4	Mr. P Kalyan
3	16DEC003	VLSI Technology and Design	4	Mr D.V.Ramana
4	16DEC002	Digital design through VERILOG	4	Dr Yogash Misra
5	19EC002	DSP Processors and Architectures	4	Dr V Kanan
6	16DEC106	HDL Programming Laboratory	2	Dr J.V Suman
7	16DEC202	Term Paper	2	Dr K. Krishna Kishore

Fig. 1: Time Table M.Tech (VLSI and Embedded system Design) 1st Year I Semester -2021-2022

CLASS TIME TABLE

Department: ECE
Year & Semester: 1st Year 2nd Sem
Chief Mentor: Dr.G.Anantha Rao

Academic Year: 2022-2023
Section:
Lecture Hall No:

REV.: 01
w.e.f : 04.07.2022

Timing	Period							
	1	2	3	4	5	6	7	
Start Time	9:00 AM	9:50 AM	10:50 AM	11:40 AM	1:30 PM	2:20 PM	3:20 PM	
End Time	9:50 AM	10:40 AM	11:40 AM	12:30 PM	2:20 PM	3:10 PM	4:10 PM	
MON					16VLS012	16VLS013	16VLS016	
TUE					GAR	YM	JVS	
WED					16VLS016	16VLS012	16VLS013	
THU					JVS	GAR	YM	
FRI			16VLS202		16VLS016	16VLS013	16VLS012	
SAT			Embedded systems laboratory		JVS	YM	GAR	
					16VLS013	16VLS012	16VLS016	
					YM	GAR	JVS	
					16VLS201	16VLS201	16CSE203	16CSE203
					PKC	PKC	CSE/IT Faculty	CSE/IT Faculty
					16CSE203	16CSE203	16VLS201	16VLS201
					CSE/IT Faculty	CSE/IT Faculty	PKC	PKC
S.No	Code	Course Title	Credits	Faculty				
1	16VLS201	Embedded and Real Time Systems	4	Mr.P.KalyanChakravarthi				
2	16CSE203	Soft Computing Techniques	4	CSE Faculty				
3	16VLS012	Low Power VLSI Design	4	Dr.G.Anatha Rao				
4	16VLS013	CPLD and FPGA Architectures & Applications	4	Dr.Yogesh Misra				
5	16VLS016	Algorithms for VLSI Design Automation	4	Dr.J.Venkata Suman				
6	16VLS202	Embedded systems laboratory	2	Mr.P.KalyanChakravarthi				

Fig. 2: Time Table M.Tech (VLSI and Embedded system Design) 1st Year II Semester -2021-2022

Meeting in 'M.Tech(VLSI) _1st_Sem_ACY:2021-22'

2022-05-31 06:10 UTC

Recorded by
Salina Pooja

Channel
M.Tech(VLSI)
_1st_Sem_ACY:2021-22

Fig. 3: Online class of subject 16VLS002 Digital Design through VERILOG of M.Tech (VLSI and Embedded system Design) 1st Year I Semester



Fig. 4: Online class of subject 16VLS013 CPLD and FPGA Architectures & Applications of M.Tech (VLSI and Embedded system Design) 1st Year II Semester