GMR Institute of Technology

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SEMESTER END REGULAR/SUPPLEMENTARY EXAMINATIONS (AR23/AR21), May – 2025

U.G.	CSE/CSE-AI&ML/CSE-AI&DS/IT	Degree	Bachelor of Technology
Academic Year	2024-2025	Sem.	4th
Course Code	23CS403/21CS403	Course Title	Computer Organization and Architecture
Duration	3 Hours	Maximum Marks	70 (SEVENTY)

SECTION-I

7 x 2 = 14 Marks

1.

No.	Questions (a to g)	RBT Level	COs
a	List the different components of computer system.	Remember	1
b	Differentiate between logical AND and logical OR operations.	Remember	1
c	Divide 16 (10000) by 2 (0010).	Apply	3
d	Define Parallelism.	Remember	3
e	Write about cache memory.	Remember	4
f	Define DMA.	Remember	4
g	What is Instruction Pipeline ?	Remember	6

SECTION-II

4 x 14 = 56 Marks

No.		Questions (2 to 9)	RBT Level	COs	Marks
2	(a)	Explain instruction set architecture in detail.	Understand	1	8M
	(b)	Explain in detail about Input and Output instructions.	Understand	2	6M
		OR			
3	(a)	Write in detail about the Instruction cycle.	Understand	1	8M
	(b)	Discuss in detail about computer register instructions.	Understand	2	6M
4	(a)	Illustrate hardware and flowchart for booths algorithm.	Understand	3	8M
	(b)	Explain any 6 different addressing modes with example.	Apply	2	6M
		OR			
5	(a)	Draw the flow chart for multiplication. Perform multiplication for (-10) * (+13).	Apply	3	8M
	(b)	List the different Arithmetic and Shift Micro operation Symbols and write their description.	Understand	2	6M
6	(a)	Explain about the different types of Interrupts with an example.	Understand	4	8M
	(b)	What is programmed I/O? Explain its working with the help of a diagram. Compare it with interrupt-driven I/O and DMA.	Understand	5	6M
		OR			
7	(a)	Explain the basic structure of MIPS architecture. Describe the different types of MIPS instructions with examples.	Understand	4	8M
	(b)	Explain the different types of memory in a computer system. Discuss how do they work together in the memory hierarchy?	Understand	5	6M
8	(a)	Describe about instruction level parallelism.	Understand	6	8M
	(b)	Write about pipelined data path and control.	Understand	5	6M
		OR			
9	(a)	What are data hazards and control hazards in pipelined processors? Explain how these hazards are handled.	Understand	6	8M
	(b)	Differentiate between a single processor and a parallel processor? Explain their working and advantages.	Understand	5	6M

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