GMR Institute of Technology
An Autonomous Institute Affiliated to JNTU-GV

GMRIT Training Tomorrow's Engineers Today

1.1.3 (A) Syllabus copy of the courses highlighting Focus on Employability/Entrepreneurship/ Skill development along with their course outcomes

Department of Electronics & Communications Engineering

INDEX

Department of Electronics and Communication Engineering

Minimum Credits to be earned: 160 (for Regular Students)
127 (for Lateral Entry Students)

No	Course Code	Course	POs	Contact Hours			
				L	T	P	C
First Semester							
1	21HSX01	Communicative English	9,10, 12	2	-	-	2
2	21MAX01	Engineering Mathematics I	1,2,3,12	3	-	-	3
3	21PYX01 21CYX01	Engineering Physics / Engineering Chemistry	1,2,12 / 1,6,7,12	3/3	-	-	3/3
4	21BEX01 21BEX06	Basics of Engineering / IT Workshop	1,3,6,7,9,11,12/1,12	3/ -	-	-/ 3	3/1.5
5	21BEX02	Problem Solving and Programming Skills	1, ,2,3,12	3	-	-	3
6	21BEX03	Problem Solving and Programming Skills Lab	2,3,4,12	-	-	3	1.5
7	21BEX04/ 21BEX05	Engineering Drawing / Engineering Workshop	1,5,10,12/1,9,10,12	-	-	3/3	1.5/1.5
8	21PYX02/ 21CYX02	Engineering Physics Lab /Engineering Chemistry Lab	4,9,11/1,3,6,7,12	-	-	3/3	1.5
9	21HSX02/-	Communicative English Lab/-	9,10,12	-	-	3/-	1.5/-
			Total	**14/11**	**0**	**12/12**	**20/17**
Second Semester							
1		Language Elective	10,12	2	-	-	2
2	21MAX02	Engineering Mathematics II	1,2,3,12	3	-	-	3
3	21CYX01/ 21PYX01	Engineering Chemistry /Engineering Physics	1,3,6,7,12/4,9,11	3/3	-	-	3/3
4	21BEX01/ 21BEX06	Basics of Engineering/ IT Workshop	1,3,6,7,9,11,12/1,12	-/3	-	3/-	1.5/3
5	21BEX07	Python Programming	1,2,3,12	3	-	-	3
6	21BEX08	Python Programming Lab	2,3,4,5,12	-	-	3	1.5
7	21BEX05/ 21BEX04	Engineering Workshop / Engineering Drawing	1,9,10,12/1,5,10,12	-	-	3/3	1.5/1.5
8	21CYX02/ 21PYX02	Engineering Chemistry Lab/Engineering Physics Lab	1,3,6,7,12/4,9,11	-	-	3/3	1.5/1.5
9	-/21HSX02	-/Communicative English Lab	9,10,12	-	-	-/3	-/1.5
			Total	**11/14**	**0**	**12/12**	**17/20**
Third Semester							
1	21MA301	Complex Variables	1,2,3, PSO2	3	-	-	3
2	21EC301	Electronic Devices and Circuits	1,2,3,PSO1	3	-	-	3
3	21EC302	Linear Circuit Analysis	1,2,4,5, PSO1	3	-	2	4
4	21EC303	Logic Circuit Design	1,2,3, PSO1	3	-	-	3
5	21EC304	Random Variables and Stochastic Processes	1,2, 3,PSO2	3	-	-	3
6	21EC305	Signals & Systems	1,2,4,5, PSO2	3	-	2	4

7	21EC306	Electronic Devices and Circuits Lab	1, 2, 4, PSO1	-	-	3	1.5
8	21EC307	Logic Circuit Design Lab	1, 2, 4, 5, PSO1	-	-	3	1.5
9	21ESX01	Employability Skills I	1,2,5,8,10,12	-	-	2	-
10	21HSX11	CC & EC Activities I	6,7,9,10	-	-	1	-
			Total	**18**	**0**	**13**	**23**
Fourth Semester							
1	21CSE01	Object Oriented Programming	1,2, 3,5	3	-	-	3
2	21EC401	Analog and Digital Communications	1,2, 3,PSO2	3	-	-	3
3	21EC402	Analog Electronic Circuits	1, 2, 4,5, PSO1	3	-	2	4
4	21EC403	Electromagnetic Fields and Waves	1,2, 3,PSO2	3	-	-	3
5	21EC404	Linear Control Systems	1, 2, PSO1, PSO2	3	-	-	3
6	21CSE02	Object Oriented Programming Lab	1,2,4,5	-	-	3	1.5
7	21EC405	Analog and Digital Communications Lab	1, 2, 4,5, PSO2	-	-	3	1.5
8	21ESX01	Employability Skills I	1,2,5,8,10,12	-	-	2	2
9	21HSX11	CC & EC Activities I	6,7,9,10	-	-	1	1
			Total	**15**	**0**	**11**	**22**
Fifth Semester							
1	21EC501	Linear and Digital IC Applications	1,2,3, PSO1	3	-	-	3
2	21EC502	Microprocessors and Microcontrollers	1, 2, 3, 4, 5, PSO1	3	-	2	4
3	21EC503	VLSI Design	1, 2,3, 4, 5, PSO1	3	-	2	4
4	21EC504	Antennas and Microwave Engineering	1,2,3, PSO2	3	-	-	3
5		Elective I (Professional Elective)		3	-	-	3
6		Elective II (Open Elective I)		3	-	-	3
7	21EC505	Linear IC Applications Lab	1,2,3, 4, PSO1	-	-	3	1.5
8	21TPX01	Term Paper	1,4,9,10,12,PSO1,PSO2	-	-	3	1.5
9	21ESX02	Employability Skills II	1,2,5,8,10,12	-	-	2	-
10	21HSX12	CC & EC Activities II	6,7,9,10	-	-	1	-
11	21SIX01	Summer Internship I	1,2,8,10,12	-	-	-	1
			Total	**18**	**0**	**13**	**24**
Sixth Semester							
1	21HSX10	Engineering Economics and Project Management	1,10,11,12	3	-	-	3
2	21EC601	Cellular and Mobile Communications	1,2,3, PSO2	3	-	-	3
3	21EC602	Digital Signal Processing	1,2, 3,PSO2	3	-	-	3
4		Elective III (Professional Elective)		3	-	2	4
5		Elective IV (Open Elective II)		3	-	-	3
6	21EC603	Digital Signal Processing Lab	1,2,4,5, PSO2	-	-	3	1.5
7	21MPX01	Mini Project	ALL	-	-	3	1.5
8	21ESX02	Employability Skills II	1,2,5,8,10,12	-	-	2	2
9	21HSX12	CC & EC Activities II	6,7,9,10	-	-	1	1
10	21ATX01	Environmental Studies	1,6,7,12	-	-	-	-
11	21ATX02	Human Values and Professional Ethics	----------	-	-	-	-

12	21ATX----	Audit Course	----------	-	-	-	-
			Total	**15**	**0**	**11**	**22**
Seventh Semester							
1	21PWX01	Project Work	ALL	-	-	16	8
2		Elective V (Professional Elective)		3	-	-	3
3		Elective VI (Professional Elective)		3	-	-	3
4		Elective VII (Open Elective III)		3	-	-	3
5	21SIX02	Summer Internship II	1,2,8,10,12	-	-	-	1
			Total	**9**	**0**	**16**	**18**
Eighth Semester							
1	21FIX01	Full Semester Internship (FSI)	1,2,5,8,9,10, PSO1, PSO2	-	-	**-**	8
2		Elective VIII (Professional Elective)		-	-	**-**	3
3		Elective IX (Open Elective IV)		-	-	**-**	3
			Total	**0**	**0**	**-**	**14**

List of Electives

No.	Course Code	Course	POs	Contact Hours			
				L	T	P	C
Language Electives							
1	21HSX03	Advanced Communicative English	9,10,12	2	-	-	2
2	21HSX04	Communicative German	10,12	2	-	-	2
3	21HSX05	Communicative French	10,12	2	-	-	2
4	21HSX06	Communicative Japanese	10,12	2	-	-	2
5	21HSX07	Communicative Spanish	10,12	2	-	-	2
6	21HSX08	Communicative Korean	10,12	2	-	-	2
7	21HSX09	Communicative Hindi	10,12	2	-	-	2
Elective I							
Career Path I, II, III and Other Core Electives							
1	21ECC11	RTL Coding Techniques (Chip Design Career Path)	1, 2, 3, PSO1	3	-	-	3
2	21ECC21	Data Acquisition System (Embedded System Design Career Path)	1, 2, 3,PSO1	3	-	-	3
3	21ECC31	Information Theory and Coding Techniques (Communication and Signal Processing)	1, 2, 3,PSO2	3	-	-	3
4	21IT304	Database Management Systems	1, 2, 3	3	-	-	3
5	21CS303	Data Structures	1, 2	3	-	-	3
6	21CS403	Computer Organization and Architecture	1,2	3	-	-	3
Elective III							
Career Path I, II, III and Other Core Electives							
1	21ECC12	ASIC Verification using system Verilog (Chip Design Career Path)	1, 2, 3,4,5, PSO1	3	-	2	4
2	21ECC22	Embedded System Design and IoT (Embedded System Design Career Path)	1, 2, 3, 4, 5, PSO1	3	-	2	4
3	21ECC32	Image processing (Communication and Signal Processing)	1, 2,4,5, PSO2	3	-	2	4
4	21EC004	Virtual Instrumentation	1, 2, 4, 5, PSO2	3	-	2	4
5	21EC005	Cryptography and Network Security	1, 3, 4, 5, PSO1	3	-	2	4
6	21CS503	Computer Networks	1,2,4,5,PSO1,PSO2	3	-	2	4
Elective V							
Career Path I, II, III and Other Core Electives							
1	21ECC13	Analog and mixed signal VLSI design (Chip Design Career Path)	1, 2, 3, PSO1	3	-	-	3
2	21ECC23	Real Time Operating Systems (Embedded System Design Career Path)	1,2, 3,PSO1	3	-	-	3
3	21ECC33	Multimedia communications (Communication and Signal Processing)	1, 2, 3,PSO2	3	-	-	3
4	21EC006	Wireless Sensor Networks	1, 2, PSO1, PSO2	3	-	-	3
5	21IT403	Operating Systems	1, 12	3	-	-	3
6	21CS603	Software Engineering	4, 5, 8, 11, PSO1	3	-	-	3
Elective VI							
1	21EC007	Design for testability	1, 2, 3, PSO1	3	-	-	3
2	21EC008	Biomedical Signal Processing	1,2, 3,PSO2	3	-	-	3
3	21EC009	UHF and EHF communication systems	1, 2,3, PSO2	3	-	-	3

4	21EC010	Neural Networks and Deep Learning	1, 2, PSO1, PSO2	3	-	-	3
Elective VIII (Professional Elective)							
1	21EC012	Real-Time Systems Design and Analysis	1, 2, 3,PSO1	-	-	-	3
2	21EC013	Image Processing for Engineering Applications	1, 2, 3,PSO2	-	-	-	3
3	21EC014	Computer Architecture	1, 2,3, PSO1	-	-	-	3
Open Electives							
1	21CE001	Disaster Management	2,7	3	-	-	3
2	21EE001	Electrical Installation, Safety and Auditing	2,3,6,8	3	-	-	3
3	21ME001	Fundamentals of Optimization Techniques	1,2,3,5	3	-	-	3
4	21EC001	Sensors for Engineering Applications	1,2,6,7	3	-	-	3
5	21CS001	Fundamentals of Artificial Intelligence	1,2,3	3	-	-	3
6	21CH001	Energy Conversion and Storage Devices	1,3,6,7	3	-	-	3
7	21IT001	Fundamentals of Multimedia	3,5,7	3	-	-	3
8	21BS001	Nano Materials and Technology	1,12	3	-	-	3
9	21DS001	Fundamentals of Data Science	1,2	3	-	-	3
10	21CE002	Air Pollution and Environmental Impact Assessment	6,7,12	3	-	-	3
11	21EE002	Renewable Energy Sources	2,7	3	-	-	3
12	21ME002	Principles of Entrepreneurship	1,5,8,11	3	-	-	3
13	21EC002	Electronics for Agriculture	1,2,6,7	3	-	-	3
14	21CS002	Fundamentals of Machine Learning	2,5	3	-	-	3
15	21CH002	Industrial Safety and Hazard Management	1,2,3,6,8	3	-	-	3
16	21IT002	Fundamentals of Cloud Computing	2,6,7,8,12	3	-	-	3
17	21BS002	Advanced Numerical Techniques	1,2	3	-	-	3
18	21BS003	Functional Materials and Applications	1,7	3	-	-	3
19	21CE003	Solid Waste Management	3,7,12	3	-	-	3
20	21EE003	Fundamentals of Electrical Vehicle Technology	2,3,12	3	-	-	3
21	21ME003	Industrial Engineering and Management	1,11	3	-	-	3
22	21EC003	Interfacing and Programming with Arduino	1,2,3,6	3	-	-	3
21	21CS003	Data Science for Engineering Applications	2,3,4	3	-	-	3
24	21CH003	Industrial Ecology for Sustainable Development	2,6,7	3	-	-	3
25	21IT003	Fundamentals of Mobile Computing	1,7	3	-	-	3
26	21BS004	Advanced Materials of Renewable Energy	1,7	3	-	-	3
27	21BS005	Applied Linear Algebra for Engineers	1,12	3	-	-	3
28	21CE019	Green Buildings	1,7,12	3	-	-	3
29	21EE017	Sustainable Energy	2,3,12	3	-	-	3
30	21ME019	Total Quality Management	1,11	3	-	-	3
31	21EC011	Communication Technologies	1,2,3,6	3	-	-	3
32	21CS020	Applications of Artificial Intelligence	2,3,6,7	3	-	-	3
33	21CH016	Green Technologies	2,6,7	3	-	-	3
34	21IT015	Human Computer Interaction	1,7	3	-	-	3
35	21BS006	Handling of Industrial waste and waste water	1,7	3	-	-	3
36	21OE001	Robotics and Automation	5,6,7	3	-	-	3
37	21OE002	Introduction to IoT	1,2	3	-	-	3
38	21OE003	Fundamentals of Image processing	1,2,3,6	3	-	-	3
39	21OE004	Fundamentals of Data Acquisition systems	1,2	3	-	-	3
40	21OE005	Airport Operations Management	2,4,11,12	3	-	-	3
41	21OE006	Fundamentals of Embedded Systems	1,2	3	-	-	3

42	21OE007	Remote Sensing and GIS	1,2,5,7,10	3	-	-	3
43	21OE008	Big Data Analytics	1,7	3	-	-	3
44	21OE009	Fundamentals of Cyber Security	3,6,8	3	-	-	3
45	21OE010	Smart Cities	7,12	3	-	-	3
46	21OE011	Nano Materials and Thin Film Technology	1,12				
47	21CSMC1	Cloud computing	2,3	3	-	-	3
48	21CSMC2	Ethical Hacking	1,2,3	3	-	-	3
49	21CSMC3	Fundamentals of Web Development	2,3,5	4	-	-	4
50	21OE012	Business Intelligence & Analytics	2,3,5	3	-	-	3
51	21OE013	Introduction To Industry 4.0 And Industrial IoT	2,3	3	-	-	3
52	21OE014	Natural Language Processing	2,3	3	-	-	3
Audit Course							
1	21AT001	Communication Etiquette in Workplaces	-	-	-	-	-
2	21AT002	Contemporary India: Economy, Policy and Society	-	-	-	-	-
3	21AT003	Design The Thinking	-	-	-	-	-
4	21AT004	Ethics and Integrity	-	-	-	-	-
5	21AT005	Indian Heritage and Culture	-	-	-	-	-
6	21AT006	Intellectual Property Rights and Patents	-	-	-	-	-
7	21AT007	Introduction to Journalism	-	-	-	-	-
8	21AT008	Mass Media Communication	-	-	-	-	-
9	21AT009	Science, Technology and Development	-	-	-	-	-
10	21AT010	Social Responsibility	-	-	-	-	-
11	21AT011	The Art of Photography and Film Making	-	-	-	-	-
12	21AT012	Gender Equality for Sustanibity	-	-	-	-	-
13	21AT013	Women in Leadership	-	-	-	-	-
14	21AT014	Introduction to Research Methodology	-	-	-	-	-
15	21AT015	Climate Change and Circular Economy	-	-	-	-	-
B. Tech. (Honors)							
Domain I VLSI Circuit Design and Verification							
01	21ECH11	System on Chip Design	1,2,PSO1	4	-	-	4
02	21ECH12	CMOS Logic Circuit Design	1, 2, 3, PSO1	4	-	-	4
03	21ECH13	Low Power VLSI Design	1, 2, 3, PSO1	4	-	-	4
04	21ECH14	VLSI Fabrication Technology	1,2,3, PSO1	4	-	-	4
Domain II Robotics and Automation							
01	21ECH21	Advanced Controllers	1, 2, 3, PSO1	4	-	-	4
02	21ECH22	Robots and Control	1, 2, 3, PSO1	4	-	-	4
03	21ECH23	Industrial Automation	1, 2, PSO1, PSO2	4	-	-	4
04	21ECH24	Distributed Embedded systems	1, 2, 3, PSO1	4	-	-	4
Domain III Cognitive Radio Networks							
01	21ECH31	Optical Communications	1, 2, PSO2	4	-	-	4
02	21ECH32	MIMO Wireless Communications	1,2,3, PSO2	4	-	-	4
03	21ECH33	Software Defined Radio	1, 2,PSO2	4	-	-	4
04	21ECH34	Wireless and Mobile Networks	1, 2, PSO1	4	-	-	4
Domain IV Multimedia Signal Processing							
01	21ECH41	Optimization Techniques	1, 2,PSO1, PSO2	4	-	-	4
02	21ECH42	Audio Signal Processing	1,2,3,PSO2	4	-	-	4
03	21ECH43	Statistical Signal Processing	1,2,3,PSO2	4	-	-	4
04	21ECH44	Computer Vision	1,2,PSO2	4	-	-	4
B. Tech. (Minors)							
Electronics and Communications Engineering							

01	21ECM01	Electronic Devices and Linear ICs		4	-	-	4
02	21ECM02	Fundamentals of Digital Signal Processing		4	-	-	4
03	21ECM03	Fundamentals of VLSI Design		4	-	-	4
04	21ECM04	Digital Design with Verilog		4	-	-	4
05	21ECM05	Principles of Communications		4	-	-	4

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21EC501 Linear and Digital IC Applications

3 0 0 3

Course Outcomes

1. Illustrate the characteristics and internal structure of Operational amplifier
2. Classify various configurations of differential amplifiers
3. Differentiate linear and non-linear applications of operational amplifier
4. Design various types of analog filters
5. Outline the operation and applications of IC 555 time and PLL
6. Compute the working of various types of ADCs and DACs

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5	PSO_1
1	2	-	-			2
2	2	-	-			2
3	3	2	2			3
4	3	2	2	2	2	3
5	3	2	2	2	2	3
6	3	2	-	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Integrated Circuit

DC and AC analysis of dual input balanced output differential amplifier, Properties of other differential amplifier configurations, DC coupling and cascade differential amplifier stages, current mirror, Level Translator, Constant current Bias circuit. Integrated circuits classification, package types, Op-Amp Block diagram,741 OP-AMP ideal and practical, DC and AC characteristics, 741 OP-AMP and its features, frequency response of OP-AMP Frequency compensation technique.

Temperature ranges, FET input OP-Amps **13 Hours**

Unit II

Applications of OP-AMPS

Inverting and non-inverting amplifier, adder, subtractor, integrator, differentiator, difference amplifier, instrumentation amplifier, V-I converters, I-V converters , comparators, Schmitt Trigger, Multivibrators, square wave and Triangular wave generators, RC phase shift oscillator, Log and antilog amplifiers.

Buffers, precision rectifiers **11 Hours**

Unit III

Analog filters, 555 Timers and phase locked loop

Introduction, Butterworth filters-first order, second order LPF, HPF filters. Band pass, Band reject and all pass filters, Introduction to 555 Timer, functional diagram, Monostable and Astable operations and applications, Schmitt Trigger, VCO, PLL: Introduction, Block schematic, principles and description of individual blocks,565 PLL .applications of PLL: Frequency multiplication, frequency translation.

AM, FM and FSK demodulators using PLL. **12 Hours**

Unit–IV

D/A & A/D Converters, IC Regulators

Introduction, , Sample & Hold amplifiers, Weighted resistor DAC, R-2R Ladder DAC, Inverted R-2R DAC Parallel comparator type ADC, counter type ADC, successive approximation ADC and Dual slope ADC, IC regulators 78XX, 79XX, LM723,LM317, LM337, introduction to logic families (RTL, DTL, TTL, ECL).

DAC and ADC specifications **12 Hours**

Total: 48 Hours

Textbook (s)

1. Ramakanth A. Gayakwad, Op-Amps & Linear ICs, 3rd edition, PHI, 2002.
2. D. Roy Chowdhury, Linear Integrated Circuits, New Age International (p) Ltd, 2nd Edition, 2003.
3. Venkat Rao K, Rama Sudha K and Manmadharao G, Pulse and Digital Circuits, Pearson Education, 1st edition, 2012.

Reference (s)

1. Sergio Franco, Design with Operational Amplifiers & Analog Integrated Circuits, McGraw Hill, 2001.
2. Donald A Neamen, Electronic circuit analysis and design, Tata McGraw Hill, 2nd edition,2002.
3. R.F.Coughlin & Fredrick Driscoll, Operational Amplifiers & Linear Integrated Circuits, PHI, 6th edition, 2002.

21EC502 Microprocessors and Microcontrollers

3 0 2 4

Course Outcomes

1. Assess the architecture and instructions of 8086 microprocessor
2. Demonstrate the application of addressing modes
3. Execute assembly language programs based on microprocessor
4. Assess the architecture and instructions of 8051 microcontroller
5. Execute assembly language programs based on microcontroller
6. Implement the interfacing of peripherals with microcontroller

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5	PSO_1
1	2	-	-	-	-	2
2	3	2	2	2	3	3
3	3	2	2	-	3	2
4	2	-	-	-	-	2
5	3	2	2	2	3	3
6	3	2	3	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

8086 Microprocessors and Assembly Language Programming

Introduction to microcomputer, evolution of processors and semiconductor memories (RAM, ROM, EPROM, EEPROM), Architecture of 8086 microprocessor, Register organization of 8086, Pipelining concept, Memory segmentation, Addressing Modes.

Instruction Set and Programming: Instruction set of 8086 microprocessor: Data transfer instructions, Arithmetic instructions, Logical Instructions, String instructions, Stack related instructions, Branching instructions, Assembler directives.

Data transfer instructions of 8085 microprocessor, Architecture of 8085 microprocessor

Practical Components

1. Data transfer program using different addressing modes in assembly language programming.
2. Perform arithmetic operations on 8 bit and 16 bit numbers in assembly language programming.
3. Data transfer program using string instruction in assembly language programming.
4. Program for data conversion in assembly language programming.

14+8 Hours

Unit II

8086 Operational Modes and Memory Interfacing

Minimum and Maximum mode operations of 8086 with timing diagrams, Procedures and macros, Stack Structure of 8086, Static RAM Interfacing, Interfacing of 8255 Programmable Peripheral Interface with 8086 microprocessor.

Dynamic RAM, Direct memory access

Practical Components

1. Write assembly language program using procedure.
2. Write assembly language program using macro.
3. Program to reject negative numbers from a series of bytes.

10+6 Hours

Unit III

8051 Microcontroller

Comparison between microprocessor and microcontroller, 8051 family microcontroller, RAM architecture of 8051, Integrated Development Environment (IDE), Pin description of 8051 microcontroller, Machine cycle. Addressing Modes, Instruction set of 8051: Data transfer instructions, Arithmetic instructions, Logical Instructions, Stack related instructions, Branching instructions. Programing and Applications of Timers, Interrupts, Universal Asynchronous Receiver Transmitter (UART).

External memory interfacing with 8051 microcontroller, various constituents of hex file

Practical Components

1. Perform Arithmetic operations on 8bit numbers in assembly language programming using 8051 microcontroller.
2. Program to toggle the LED.
3. Programming and interfacing of traffic light logic.
4. Program to generate square wave using interrupts.

12+8 Hours

Unit IV

Interfacing with 8051 microcontroller with External Peripherals

Interfacing with 8051 microcontroller with: Keypad matrix, LCD, Seven segment displays, L293D Motor driver, Stepper motor, Analog to Digital Converter (804), Digital to Analog Converter (808), introduction to CISC architecture, RISC architecture and ARM processor.

Interfacing of temperature sensor (LM 35) with 8051, interfacing of relay with 8051

Practical Components

1. Programming and interfacing of the key pad matrix.
2. Programming and interfacing of seven-segment display.
3. Programming and interfacing of the LCD.
4. Programming and interfacing of the relay.
5. Programming and interfacing of the dc/Stepper motor.

12+10 Hours

Total: 48+32 Hours

Textbook (s)

1. A.K. Ray & K. M Bhurchandi, Advanced Microprocessors & peripherals, Tata McGraw-Hill, 3rd Edition, 2012
2. Muhammad Ali Mazidi, Janice Gillispie Mazidi and Rolin D. McKinlay, The 8051 Micro controller and Embedded systems: using assembles and C, Pearson, 2nd Edition,2007

Reference (s)

1. D.V.Hall, Microprocessor and Interfacing, Tata McGraw Hill Publishing Company, 2nd Edition 2006
2. N. Sentil Kumar, M Sarvanan, S Jeevananthan, Microprocessors and Microcontrollers, Oxford University Press, 1st Edition, 2010
3. Kenneth J Ayala, The 8051 Microcontroller Architecture, Programming and Applications, Thomson Publishers, 3rd Edition, 2004

21EC503 VLSI Design

Course Outcomes **3 0 2 4**

1. Explain the basic MOSFET circuits operation and MOS fabrication Process
2. Implement the layout diagrams for CMOS circuits
3. Assess the effects of parasitics and Scaling of MOS circuits
4. Interpret the operation of basic analog and digital MOSFET circuits
5. Implement the Digital and Analog circuits with Full-custom and Semi-custom design flows.
6. Interpret the VLSI implementation flows and the basics of VLSI testing

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5	PSO_1
1	2	-	-	2	3	2
2	3	2	2	2	3	3
3	3	2	2	2	3	3
4	2	-	-	2	3	2
5	3	2	2	2	3	3
6	2	-	-	2	3	2

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

Unit I

Introduction and basic electrical properties of MOS circuits: Introduction to VLSI Design Flow, Introduction to IC technology, I_{ds} versus V_{ds} Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor conductance, Output Conductance and Figure of Merit. Fabrication process: nMOS, pMOS and CMOS. Alternate pull up forms in inverter circuits, Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter, basic current mirror, CMOS Inverter, Latch-up in CMOS circuits.

Static power dissipation, Dynamic Power dissipation in CMOS circuits

Practical components

1. Simulation of nMOS inverter
2. Functional verification of CMOS inverter
3. Functional verification of AND gate using pass transistor
4. Perform the simulation of the basic current mirror

13+8 Hours

Unit II

Basics of VLSI: Driving large capacitive loads, Cascaded CMOS inverters for delay optimization, Wiring Capacitances, Stick Diagrams, Design Rules and Layout, Layout Diagrams for MOS circuits, Sheet resistance, Gate capacitance, The Delay Unit, Inverter Delays, Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling: performance improvement by CMOS scaling.

Drain Induced Barrier Lowering (DIBL) effect, Sub threshold conduction

Practical components

1. Layout design of CMOS inverter
2. Perform the DRC and LVS for the CMOS inverter Layout
3. Perform the RC extraction for CMOS inverter
4. Compute the delay of CMOS inverter after the RC extraction

11+8 Hours

Unit III

Basic Digital and Analog Circuits: Static CMOS logic, Cascode Voltage Switch Logic, Transmission Gates, Pass Transistor Logic, Dynamic logic, Domino logic, Metastability, setup time, hold time, Small signal Modeling of transistor, body bias effect, biasing styles of MOSFET FET amplifiers, single stage amplifier with resistive load, Common Source amplifier, Common Drain amplifier, Common Gate amplifier.

CMOS full adder, Clocked CMOS registers

Practical components

1. Design and simulation of Half adder using transmission gate logic
2. Simulate a one transistor Common Source amplifier with resistive load
3. Design and simulation of Half adder using pass transistor
4. Simulate a one-transistor common drain amplifier

12+8 Hours

Unit IV

VLSI Implementation Strategies and Testing:

Introduction, ASIC Design flow, types of ASICs- Full custom, Standard cell based Asics, Gate array based ASICs, FPGAs, FPGA design flow, Basic FPGA Design Structure FPGA Programming Technologies: SRAM, EPROM, EEPROM; Introduction to testing, Manufacturing test principles, Design for testability (DFT) - Adhoc testing, Scan design, Built in self-test (BIST)

Xilinx3000Series, Boundary scan

Practical components

1. Design and ASIC Implementation of 4:1 MUX
2. Design and FPGA Implementation of 2:4 Decoder
3. Design and FPGA Implementation of a D-Latch
4. Perform the ASIC implementation of a 4-bit counter

12+8 Hours

Total: 48+32 Hours

Textbooks:

1. Kamran Eshraghian, Douglas ,A. Pucknell And Sholeh Eshraghian, Essentials of VLSI Circuits and Systems, , Prentice-Hall of India Private Limited, 2005 Edition.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2003
3. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits, Pearson Education, 2nd edition,2016.
4. Weste and Eshraghian, Principles of CMOS VLSI Design, Pearson Education, 3rdEdition, 1999
5. Michael john Sebastian smith, Application specification integrated circuits, Addition Wesley,1st edition,1997

References:

1. John P. Uyemura, ,Introduction to VLSI Circuits and Systems, John Wiley & Sons, reprint 2009.
2. Vinod Kumar Khanna, Integrated Nanoelectronics: Nanoscale CMOS, Post-CMOS and Allied Nanotechnologies, Springer India, 1st edition, 2016.
3. Michael John Sebastian Smith, Application Specific Integrated Circuits, Addison-Wesley, 1997.

21EC504 Antennas and Microwave Engineering

3 0 0 3

Course Outcomes

1. Illustrate parameters of an antenna and antenna arrays
2. Implement antenna arrays
3. Design an antenna for given specifications
4. Justify modes of rectangular waveguide and the S-parameters of waveguide components
5. Summarize operation of microwave tubes
6. Interpret microwave measurements

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_2
1	2	-	-		2
2	3	2	-		3
3	3	2	2		3
4	3	2	-	2	3
5	2	-	-	2	2
6	2	-	2	2	2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Antenna Fundamentals & Uniform Linear Arrays

Radiation Mechanism: Single wire, Two wire, Dipoles, Current Distribution on a thin wire antenna, Antenna Parameters: Radiation Patterns, Patterns in Principal Planes, Main Lobe and Side Lobes, Beam width, Beam Area, Bandwidth, input impedance, Radiation Intensity, Beam Efficiency, Directivity, Gain, Antenna Apertures, Antenna efficiency, Antenna regions, Friis Transmission equation.

Antenna arrays: Different cases of 2 element arrays, Principle of Pattern Multiplication, N element Uniform Linear Arrays: Broadside and End fire Arrays. Introduction to LiDar.

Binomial array and it's applications **13 Hours**

Unit II

Arrays with Parasitic Elements and Special Antennas

Arrays with Parasitic Elements: Yagi Uda Arrays, Folded Dipoles & their characteristics, Paraboloidal Reflectors: Geometry, characteristics, types of feeds, F/D Ratio, Spill Over, Back Lobes, Aperture Blocking, Off-set Feeds and Cassegrain Feeds.

Helical Antennas: Significance, Geometry, basic properties, Design considerations for monofilar helical antennas in Axial Mode and Normal Modes (Qualitative Treatment), Horn Antennas - Types, Optimum Horns, Design Characteristics of Pyramidal Horns, Design of Rectangular and Circular Microstrip Patch antenna, Log Periodic antennas - Introduction, Planar wire surfaces.

Applications of microstrip patch antenna and Lens antennas **11 Hours**

Unit III

Waveguides and Wave Guide Components

Introduction: Microwave Spectrum, advantages and applications of microwaves, Rectangular waveguides- TE/TM mode analysis, Expressions for Fields, Characteristic Equation and Cut-off Frequencies, Dominant and Degenerate Modes, Mode Characteristics: Phase and Group Velocities.

Scattering Matrix: Significance, Properties, S Matrix Calculations for multi-port Junctions - E plane and H plane Tees, Magic Tee, Directional Coupler, Faraday rotation devices- Gyrator, Isolator, Circulator.

Hybrid Rings and rat race junction

14 Hours

Unit IV

Microwave Tubes and Microwave Measurements

Limitations and Losses of conventional tubes at microwave frequencies, Two Cavity Klystron - Velocity Modulation and Applegate Diagram, Bunching Process. Reflex Klystron - Applegate Diagram and Principle of working, Magnetron - 8-Cavity Cylindrical Travelling Wave Magnetron.

Microwave Bench- Different Blocks and their Features, Precautions, Microwave Power Measurement: Bolometer Method, Measurement of Attenuation, Frequency, VSWR, Impedance Measurement.

Applications Gunn Diode and Impatt diode

10 Hours

Total: 48 Hour

Textbook (s)

1. C.A Balanis, Antenna Theory, John Wiley & Sons, 3rd Edition. 2016
2. John D Krauss, Ronald J Marhefka, Ahmad S Khan, Antennas for all applications, Tata McGraw-Hill, 3rd Edition, 2009
3. K. D. Prasad, Antennas & Wave Propagation, Satya Prakashan, New Delhi, 3rd Edition, 2011
4. Samuel Y. Liao, Microwave Devices and Circuits, Pearson education, 3rd Edition, 2007
5. Pozar, Microwave Engineering, Wiley publishers, 4th Edition, 2012

Reference (s)

1. E.C. Jordan and K.G. Balmain, Electromagnetic Waves and Radiating Systems, PHI, 2nd Edition, 2011
2. John D Kraus, Antennas, Tata McGraw-Hill, 2nd Edition, 2001
3. R.E. Collin, Foundations for Microwave Engineering, IEEE Press, John Wiley, 2nd Edition, 2000
4. M. Kulkarni, Microwave and Radar Engineering , Umesh Publications, 4 th Edition, 2010

21ECC11 RTL Coding Techniques

3 0 0 3

Course Outcomes:

1. Interpret the RTL design guidelines and synthesis of procedural blocks
2. Illustrate the Verilog RTL coding techniques
3. Use the RTL design techniques in HDL coding of digital circuits
4. Demonstrate the RTL design techniques for the implementation of sequential and combinational blocks
5. Perform the RTL coding at block level for a digital system architecture
6. Interpret the control path and data path for complex digital circuits

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_1
1	2	-	-		2
2	2	-	-		2
3	3	2	2		3
4	3	2	2	2	3
5	3	2	2	2	3
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

RTL Coding Techniques-I

Introduction to Verilog & Modelling Styles, RTL Design Guidelines, Parallel Versus Priority Logic, Blocking Assignments and Event Queue, Blocking Assignments and multiple "always" blocks, Blocking Assignments in the same "always" block, ordering of non-blocking assignments, Continuous versus Procedural Assignments, Combinational Loops in Design.

RTL code for Subtraction using 2's complement, ALU

12 Hours

Unit II

RTL Coding Techniques-II

Sequential statements - 'case' with missing 'default', 'if-else' with missing 'else', Logical Equality versus Case Equality, Incomplete Sensitivity List, Unintentional Latches in the Design, if-else versus case statements, Arithmetic Resource Sharing, Asynchronous Reset D flip-flop, Synchronous Reset D flip-flops, Gated Clocks, Clock Enables

RTL code for 2 to 4 decoder using conditional statement, Synthesize the RTL for 4 to 1 Mux missing else

12 Hours

Unit III

RTL Coding Practice

State Machines and Optimization, Moore Machine, Mealy Machine, Sequence Detectors using FSM's, Design without Pipelining, Design with Pipelining, Synchronous Counters: Up-Down Counter, Ring Counter, Johnson Counter, Asynchronous Counter: Ripple Counter; Structured design of nibble adder, Multiplexer, Decoder

RTL code for the encoder, decoder, shift registers

12 Hours

Unit IV

RTL Coding for Digital Architectures

Tri-State Bus, Bus Arbitration, Static Arbitration, Bidirectional Data Transfer, RTL design for~~,~~ Single-Port RAM, Dual-Port RAM**,** RTL design for Serial adder: Control path and Data path

SDRAM Memory Controller, DDR Memory Controller

12 Hours

Total: 48 Hours

Textbook (s)

1. Vaibbhav Taraate, Advanced HDL Synthesis and SOC Prototyping (RTL Design Using Verilog), Springer Nature Singapore Pte Ltd., 2019
2. Vaibbhav Taraate, Digital Logic Design Using Verilog Coding and RTL Synthesis, Springer Nature Singapore Pte Ltd., 2016
1. J Bhasker, A Verilog HDL Primer, Star Galaxy Publishing, 3rd Edition, 2018

Reference (s)

1. Michael D. Ciletti, Advanced Digital Design with the Verilog, Prentice-Hall of India Private limited, 2nd Edition, 2005

21ECC21 Data Acquisition System

3 0 0 3

Course Outcomes

1. Illustrate various digital data acquisition systems
2. Assess various data transfer techniques
3. Demonstrate the working principle of serial interface
4. Demonstrate the working principle of various digital instruments
5. Interpret various signal condition techniques
6. Outline various Remote data Acquisition techniques

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_1
1	2	-	-		2
2	3	2	2		3
3	3	2	2		3
4	3	2	2	2	3
5	2	-	-	2	2
6	3	3	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Data Acquisition systems & control

Use of signal conditioners, scanners, signal converters, recorders, display devices, A/D & D/A circuits in digital data acquisition, Instrumentation systems: Types of Instrumentation systems, Components of an analog Instrumentation Data – Acquisition system. Multiplexing systems, Uses of Data Acquisition Systems, Use of Recorders in Digital systems, Digital Recording systems, Modern Digital Data acquisition system, Analog Multiplexed operation, operation of sample Hold circuits.

sample & hold circuits- specifications and design considerations.

12 Hours

Unit II

Data Transfer Techniques:

Interfacing To PC: Expansion Buses- ISA Bus, EISA Bus, PCI Bus. Plug in data Acquisition and Control Boards: Functions of Plug in DAQ boards, Design of General purpose DAQ boards, Design of DAQ boards for PCI Bus. Data Acquisition using Serial Interface: Serial Interface Standards Rs 232, USB-Features of USB, USB system, USB Transfer, USB Descriptors, GPIB/IEEE-488, LAN, Universal serial bus, HART protocol, Zigbee and Bluetooth.

Foundation Field bus, ModBus

12 Hours

Unit III

Digital Instruments

Digital voltmeters (DVMs): working principle, construction, operation, salient features, range selection– Ramp type, dual slope integrating type, successive approximation type, Digital Frequency Meter: working principle, construction (block diagram), range selection and operation of, time period meter, frequency ratio meter, Recorders: The working principle, construction, operation and salient features of X-t strip chart recorder, Introduction to PLC

X-Y strip chart recorder and Magnetic type recorder. **12 Hours**

Unit IV

Signal Conditioning and DAQ Systems

Single channel and multichannel, Graphical Interface (GUI) Software for DAS, RTUs, PC-Based data acquisition system , Data logging - applications - Automobile, Aerospace Manufacturing, Environmental monitoring. Temperature Measurement using Thermistor, Thermocouple, Strain Measurement System, Interfacing Piezo electric Actuator and sensor, Interfacing Light Emitting Diode and Photo sensor, Acceleration Measurement, Function Generator, DC position servomotor control, Remote data Acquisition using Internet, Machine vision-based inspection system. IC engine data

12 Hours

Total: 48 Hours

Text Books

1. Di Paolo Emilio, Maurizio , "Data Acquisition Systems From Fundamentals to Applied Design", Springer; 2013.
2. S. Gupta, J.P. Gupta, PC Interfacing for Data Acquisition and Process Control, ISA, 1994, 2nd Edition
3. Bell David A, "Electronic Instrumentation and Measurement", PHI, Inc, New Delhi (1994).
4. Tocci Ronald J , "Digital Systems Principles and Applications", PHI, New Delhi (2002)

Reference Books

1. A. D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1st Edition, 2015.
2. R. K. Jain , "Mechanical & Industrial Measurements", Khanna pub.
3. Chennakesava R Alavala, "Principles of Industrial Instrumentation and control systems", Cengage publ.

21ECC31 Information Theory and Coding Techniques

3 0 0 3

Course Outcomes

1. Exemplify the information theory concepts and channel capacity
2. Explain various kinds of channels and Shannon theorem
3. Outline various source coding techniques
4. Demonstrate the generation and detection of error control codes
5. Summarize the channel coding techniques
6. Outline the encoding and decoding structure of convolutional codes

COs-POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_2
1	2	1			2
2	2	1			2
3	3	2	2		3
4	3	2	2	2	3
5	2	1		2	2
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Information Theory

Concept of information, Mutual information, Entropy: marginal, conditional, joint and relative entropies, relation among entropies, Mutual information, information rate, channel capacity, redundancy and efficiency of channels, Discrete channels: Symmetric channels, Binary Symmetric Channel, Binary Erasure Channel, Noise-Free Channel, Shannon's theorem.

Differential entropy, Gaussian channel

12 Hours

Unit II

Source coding

Introduction to source coding, purpose of encoding, Instantaneous codes, construction of instantaneous codes, Kraft's inequality, coding efficiency and redundancy, source coding theorem. construction of basic source codes, Shannon Fano coding, Huffman coding, Channel coding theorem for DMC (Discrete memoryless channel).

Rate-distortion function, Quantization

12 Hours

Unit III

Error Control Coding

Codes for error detection and correction: Parity check coding, Linear block codes, Error detecting and correcting capabilities, Generator and Parity check matrices, Standard array and Syndrome decoding, Hamming codes, Cyclic codes: Generator polynomial, Generator and Parity check matrices, Encoding of cyclic codes, Syndrome computation and error detection, Decoding of cyclic codes.

BCH Code, Golay code

12 Hours

Unit IV

Convolutional Codes

Encoding and state, Tree and Trellis diagrams, Maximum likelihood decoding of convolutional codes, Viterbi algorithm, Sequential decoding. Automatic repeat request(ARQ), Performance of ARQ, Probability of error and throughput, Applications: Concatenated Codes, Interleavers, The Compact Disc, Codes for Magnetic recording.

RS code, Turbo code

12 Hours

Total: 48 Hours

Textbook (s)

1. Stephen.B.Wicker, Error Control Systems for Digital Communication and storage, Prentice Hall,1995.
2. Bernard Sklar, Digital communications: Fundamentals and applications, 2nd Edition, Prentice Hall,2001.
3. Simon Haykin, Communication Systems, 4th Edition, John Wiley and Sons, 2001.

Reference (s)

1. John G.Proakis, Digital communication, 4th edition, McGraw Hill, 2001.
2. R.P. Singh, SP Sapre, Communication Systems, 3rd Edition, TMH, 2017.

21EC505 Linear IC Applications Lab

0 0 3 1.5

Course Outcomes:

1. Demonstrate the linear and nonlinear applications of OP-AMP
2. Implement Active Filters using OP-AMP
3. Assess the waveform generators using IC 741 and 555 timers
4. Implement A/D and D/A convertors
5. Assess the applications of PLL and voltage regulators
6. Implement Real time applications using OP-AMP and 555 Timer

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_1
1	3	2	2	2	3
2	3	2	2	2	3
3	3	2	2	2	3
4	3	2	2	2	3
5	3	-	2	2	3
6	3	3	3	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

List of Experiments
Students will perform minimum twelve Experiments

1. Inverting and Non-inverting Amplifiers using Op Amps.
2. Adder and Subtractor using Op Amp.
3. Comparators and voltage Follower using Op Amp.
4. OP AMP Applications–differentiator, integrator circuit
5. Square wave and Triangular waves generator using OP-AMP
6. Schmitt Trigger Circuit–Using IC 741
7. Astable multivibrator using IC 741
8. Active Filters–LPF, HPF (first order only)
9. Active Filter–Band Pass Filterand Band Reject Filter
10. IC 555 Timer– Monostable Operation Circuit
11. IC 555 Timer- Astable Operation Circuit
12. IC 565 – PLL Applications.
13. RC Phase Shift using IC-741 Op-Amp
14. Voltage Regulator using IC 78XX,79XX, 723
15. Analog to Digital Converter using OP AMP
16. Digital to Analog Converter using OP AMP

List of Augmented Experiments*

1. Design a function generator to generate sine wave, square wave and triangular wave range from 1KHz to 1MHz
2. Design a filter eliminate the noise from ECG
3. Design a Mosquito repeller by using 555 Timers
4. Design a calling bell circuit which produce Ding-Dong Soundby using 555 timer

Reading Material(s)

1. Ramakanth A. Gayakwad, Op-Amps & Linear ICs, PHI, 4th Edition. 2002.
2. D. Roy Chowdhury,Linear Integrated Circuits, New Age International (p) Ltd, 2nd Edition,2003.
3. LICA lab Manual.

21TPX01 Term Paper

0 0 3 1.5

Course Outcomes

1. Interpret the literature to link the earlier research with the contemporary technologies
2. Communicate effectively as an individual to present ideas clearly and coherently
3. Review the research findings and its correlation to the latest applications
4. Prepare documents and present the concepts clearly and coherently
5. Inculcate the spirit of enquiry for self-learning
6. Identify interdisciplinary oriented topics

COs – POs Mapping

COs	PO_1	PO_4	PO_9	PO_{10}	PO_{12}	PSO_1	PSO_2
1	-	2		-	-	3	3
2	-	-		3	3		
3	3	-		-	-	3	3
4	-	-		3	-		
5	-	-	3	-	3		
6	1	-		-	-		

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

21ESX02 Employability Skills II

0 0 2 0

Course Outcomes

1. Demonstrate oral communication and writing skills as an individual to present ideas coherently
2. Develop life skills with behavioral etiquettes and personal grooming.
3. Assess analytical and aptitude skills.
4. Develop algorithms for engineering applications.
5. Solve engineering problems using software.
6. Utilize simulation tools for testing.

COs – POs Mapping

COs	PO1	PO2	PO5	PO8	PO10	PO12
1					3	3
2				1	2	3
3	2	1		2		
4	2		2			
5	2		2			
6	2		2			

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

1. Communication Skills, Confidence and Quantitative Aptitude

Introduction to Campus Placements: Stages of Campus Placement, Skills assessed in Campus Placements & How to get ready?

Motivational Talk on Positive Thinking: Beliefs, Thoughts, Actions, Habits & Results (Success)

Resume Preparation: Resume? Templates? Mistakes to be avoided in a Resume, Steps to be followed in preparing it.(with examples)

Group Discussions (Recap): GD? Stages of a GD, Skills assessed in a GD, Blunders to be avoided, How to excel in a GD? (through Practice Sessions)

Psychometric Tests: Definition, Types of Psychometric Tests: Numerical Computation, Data Interpretation, Verbal Comprehension, Verbal Critical Reasoning and Personality Questionnaires

Exercises related to Communication: Story Writing, TAT etc

7Hours

2. Quantitative Aptitude

Square &Cube roots, Partnership, Logarithms, Progressions, Mensuration, Data Sufficiency

8 Hours

Unit II

DATA FLOW LEVEL

Continuous assignment structures, Delays, and Continuous assignments, Assignment to Vectors, Operators, Strength contention with Tri-reg Nets.

Practical Components

1. Perform the simulation of full adder and half subtractor using data flow modelling in Verilog HDL.
2. Perform the Dataflow modeling for multiplexer and demultiplexer in Verilog HDL.
3. Perform the Dataflow modelling for 3 to 8 decoder in Verilog HDL.
4. Perform the Dataflow modelling for n-bit Johnson counter in Verilog HDL.
5. Perform the simulation of parity bit generation using data flow modelling in Verilog HDL.
6. Perform the Dataflow modelling for 8-bit adder in Verilog HDL.
7. Perform the Dataflow modelling for n-bit right-to-left shift register in Verilog HDL.
8. Perform the Dataflow modelling for BCD addition in Verilog HDL.
9. Perform the Dataflow modelling for JK flipflop and T-flip flops in Verilog HDL.

15 Hours

Total 30 Hours

Textbook (s)

1. Padmanabhan, Tattamangalam R., and B. Bala Tripura Sundari. Design Through Verilog HDL. John Wiley & Sons, 2003.

Reference (s)

1. Palnitkar, Samir. *Verilog HDL: a guide to digital design and synthesis*. Vol. 1. Prentice Hall Professional, 2003.
2. Ciletti, Michael D. *Advanced digital design with the Verilog HDL*. Vol. 1. Upper Saddle River: Prentice hall, 2003.

21HSX12 CC & EC Activities II

0 0 1 0

Course Outcomes

1. Interpret and present the abstractive technical information through an activity
2. Think critically in providing solutions to the generic and common problems
3. Demonstrate the creative thinking in dealing with liberal arts
4. Instill team sprit through active engagement with the peer
5. Develop programs of common interest having social impact
6. Empower the under privileged through motivational activities

COs – POs Mapping

COs	PO6	PO7	PO9	PO10
1	-	-	-	3
2	3	2	-	-
3	3	-	-	-
4	-	-	3	-
5	3	-	-	-
6	3		-	-

21SIX01 Summer Internship I

0 0 0 1

Course Outcomes

1. Demonstrate the application of knowledge and skill sets acquired from the course and workplace in the assigned job function/s
2. Solve real life challenges in the workplace by analyzing work environment and conditions, and selecting appropriate skill sets acquired from the course
3. Articulate career options by considering opportunities in company, sector, industry, professional and educational advancement
4. Communicate and collaborate effectively and appropriately with different professionals in the work environment through written and oral means
5. Demonstrate the ability to harness resources by examining challenges and considering opportunities
6. Demonstrate appreciation and respect for diverse groups of professionals by engaging harmoniously with different company stakeholders

COs – POs Mapping

COs	PO1	PO2	PO8	PO10	PO12
1	3	-	-	-	-
2	3	-	-	-	-
3	-	-	-	-	3
4	-	-	-	3	-
5	-	2	-	-	-
6	-	-	3	-	-

21HSX10 Engineering Economics and Project Management

3 0 0 3

Course Outcomes

1. Illustrate the basic principles of engineering economics.
2. Demonstrate Cost-Volume-Profit (CVP) analysis in business decision making.
3. Implement the simple financial statements for measuring financial performance of a firm.
4. Evaluate investment proposals through various capital budgeting methods.
5. State key issues of organization, management and administration.
6. Determine the accurate project cost estimates and plan future activities.

COs – POs Mapping

CO_s	PO_1	PO_2	PO_{10}	PO_{11}	PO_{12}
1	3		2	1	2
2	3		1	2	1
3	1		3	2	2
4	1	2	3	2	1
5	2	2	1	3	1
6	1	2	2	3	1

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

Unit I

Introduction to Engineering Economics - Demand Forecasting & Cost Analysis

Concept of Engineering Economics – Types of efficiency – Managerial Economics Nature and Scope – Law of Demand – Types of Elasticity of demand.

Demand Forecasting & Cost Analysis: Demand Forecasting: Meaning, Factors Governing Demand Forecasting, Methods of Demand Forecasting (Survey and Statistical Methods) – Cost Analysis: Basic Cost Concepts, Break Even Analysis.

Factors affecting the elasticity of demand – Supply and law of Supply **11 Hours**

Unit II

Market Structures - Financial Statements & Ratio Analysis

Different type of Markets Structures – Features – Price Out-put determination under Perfect Competition and Monopoly

Financial Statements & Ratio Analysis: Introduction to Financial Accounting – Double entry system – Journal – Ledger – Trail Balance – Final Accounts (with simple adjustments) – Financial Analysis through Ratios: Interpretation of Liquidity Ratios (Current Ratio and quick ratio), Activity Ratios (Inventory turnover ratio and Debtor Turnover ratio, Creditors Turnover Ratio, Capital Turnover Ratio), Solvency Ratios (Debt- Equity ratio, Interest Coverage ratio), and Profitability ratios (Gross Profit Ratio, Net Profit ratio, Operating Ratio, P/E Ratio and EPS).

Price output determination under Monopolistic markets, Accounting concepts and conventions **13 Hours**

Unit III

Investment Decisions and Fundamentals of Management

Time Value of Money – Capital Budgeting: Meaning, Need and Techniques of Capital Budgeting

Introduction to Management: Nature – Importance – Classical Theories of Management: F.W.Taylor's and Henri Fayol's Theory – Functions and Levels of Management – Decision Making Process – Inventory Control, Objectives, Functions – Analysis of Inventory – EOQ.

Maslow & Douglas McGregor theories of Management, ABC Analysis **12 Hours**

Unit IV

Project Management

Introduction – Project Life Cycle and its Phases – Project Selection Methods and Criteria – Technical Feasibility – Project Control and Scheduling through Networks – Probabilistic Models of Networks – Time-Cost Relationship (Crashing) – Human Aspects in Project Management: Form of Project Organization – Role & Traits of Project Manager.

Sources of Long-term and Short-term Project Finance **12 Hours**

Total: 48 Hours

Textbook (s)

1. Pravin Kumar, Fundamentals of Engineering Economics, Wiley India Pvt. Ltd. New Delhi, 2015
2. Rajeev M Gupta, Project Management, 2nd Ed., PHI Learning Pvt. Ltd. New Delhi, 2014

Reference (s)

1. Panneer Selvam. R, Engineering economics, 2nd Ed.,, Prentice Hall of India, New Delhi, 2013
2. R.B.Khanna, Project Management, PHI Learning Pvt. Ltd. New Delhi, 2011
3. R. Panneer Selvam & P.Senthil Kumar, Project Management, PHI Learning Pvt. Ltd. New Delhi, 2010
   A. Aryasri, Management Science, 4th Ed., Tata McGraw Hill, 2014
   A. Aryasri, Managerial Economics and Financial Analysis, 4th Ed., Tata McGraw Hill, 2014
4. Koontz & Weihrich, Essentials of Management, 6th Ed., TMH, 2010
5. Chuck Williams and Mukherjee, Principle of Management 7th Ed., Cengage Learning, 2013

21EC601 Cellular and Mobile Communications

3 0 0 3

Course Outcomes

1. Summarize basic cellular system, handoff, frequency reuse and improving capacity of cellular system
2. Demonstrate various interference types, frequency management and channel assignment
3. Interpret various cell site and mobile antennas
4. Outline the phase difference, propagation effects in various cell coverage environments
5. Assess the Multiple access schemes and GSM digital cellular system
6. Outline the 4G cellular technology

COs–POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_2
1	2	-	-		2
2	3	2	-		3
3	2	-	-		2
4	3	2	2	2	3
5	3	2	2	2	3
6	3	2	2		3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Cellular systems and Co-Channel Interference

Introduction to cellular mobile system, Evolution of cellular systems, Performance criteria, Basic cellular system, concept of frequency reuse, Trunking and Grade of Service, Improving capacity of cellular systems: Cell splitting, Sectoring, Micro cell concept, Handoff and dropped calls. Co-Channel Interference reduction factor, Desired C/I calculation for Omni directional and directional antenna systems.

Repeaters for range extension, Picocell zone concept

12 Hours

Unit II

Frequency Planning and Cell Site- Mobile Antennas

Adjacent channel interference: Next channel and neighboring channel interference, Frequency management: Numbering, grouping of channels, channel types, channel assignment: fixed channel assignment, non-fixed channel assignment. Cell Site and Mobile Antennas: Omni directional antennas, Directional antennas for interference reduction, space diversity antennas, and Umbrella pattern antennas, minimum separation of cell site antennas, roof mounted and glass mounted antennas, high gain antennas.

Interference in heterogeneous network, Effect of lowering the antenna height

12 Hours

Unit III

Cell coverage and Multiple access schemes

Cell coverage for signal and traffic**:** Signal reflections in flat and hilly terrain, effect of human made structures, phase difference between direct and reflected paths, constant standard deviation, straight line path loss slope, general formula for mobile propagation over water and flat open area, foliage loss, near

and long distance propagation, antenna height gain, form of a point to point model, cell site antenna heights and signal coverage cells. Multiple access schemes: TDMA, FDMA and CDMA
Near and long distance propagation, WCDMA Architecture

13 Hours

Unit IV

Digital Cellular Systems and 4G Technology

Digital Cellular system: GSM Architecture, GSM operation, Channels and frame structure for GSM.
Evolution of 4G: Objectives and advantages, 4G Technologies: Ultra Wide band network, OFDM and MIMO antenna systems.
GSM protocols, Limitations of 4G

11 Hours
Total: 48 Hours

Textbook (s)

1. W.C.Y. Lee, Mobile Cellular Telecommunications, Tata McGraw Hill, 2nd Edition, 2006
2. Theodore. S. Rapport , Wireless Communications, Pearson education, 2nd Edition., 2002.
3. Gottapu Sasibhushana Rao, Mobile Cellular Communication, Pearson International, 2012

Reference (s)

1. D.Tse and P.Viswanath, Fundamentals of wirless communication, Cambridge University press, 2005.
2. W.C.Y.Lee , Wireless and Mobile Communications, McGraw Hill, 3rd Edition, 2006.

21EC602 Digital Signal Processing

3 0 0 3

Course Outcomes

1. Classify discrete time signals and systems
2. Implement Digital systems by using realization techniques
3. Implement discrete Fourier transform and Fast Fourier transform on time domain signals
4. Differentiate FIR and IIR digital filters
5. Demonstrate the concept Multirate signal processing
6. Interpret the architecture of Digital signal processors

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_2
1	2	1	1		2
2	3	3	3		3
3	3	2	2		3
4	3	3	3	2	3
5	3	2		2	3
6	2	-		2	2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Discrete–Time signals and systems

Classification of Discrete time signals, linear Time Invariant systems, stability, and causality, Linear convolution in time domain and graphical approach, Frequency Domain Representation of Discrete-Time Signals and systems. Concept of Z-transforms, Region of Convergence, properties, Inverse Z transform, Realization of Digital filter structures: Direct form-I, Direct form-II, Transposed form, Cascaded form, Parallel form
Lattice structure, Lattice-Ladder structure **12 Hours**

Unit II

Discrete–Time signals in Transform domain

Discrete Fourier Series(DFS),Discrete Time Fourier transforms(DTFT), Discrete Fourier transform(DFT), Properties of DFT , linear convolution using DFT, Circular convolution, Fast Fourier transforms (FFT) -

Radix-2 decimation in time ,decimation in frequency FFT Algorithms, Decimation in frequency FFT Algorithms, Inverse FFT, Overlap-save method, Overlap-add method
Relation between DTFT, DFS, DFT, Radix-4FFT

12Hours

Unit III
IIR &FIR Digital Filters
Analog filter approximations–Butter worth and Chebyshev, Impulse Invariant transformation, Bilinear transformation, Design of IIR Digital filters from analog filters, FIR Digital Filters: Characteristics of FIR Digital Filters, frequency response, Design of FIR Digital Filters using Window Techniques, Frequency Sampling Technique.
Comparison of IIR & FIR filters. Frequency Transformation in digital domain,

13 Hours

Unit IV
Multirate Signal Processing & TMS Processors
Multirate Processing: Decimation, interpolation, sampling rate conversion, Implementation of sampling rate conversion. Introduction to DSP processors: Overview of Digital signal processors, Von Neumann Architecture, Harvard Architecture, Multiplier Accumulator (MAC), Pipelining, Architecture of TMS320C50,Bus structure, CPU, on chip memory, on-chip peripherals
Cascading sampling rate converters, Addressing modes

11Hours
Total: 48 Hours

Textbook (s)

1. Digital Signal Processing by Sanjit K.Mitra 2nd Edition , TATA McGraw Hill
2. John G. Proakis, Dimitris, G.Manolakis ,Digital Signal Processing, Principles, Algorithms, and Applications: Pearson Education / PHI, 4th Edition, 2013.
3. Digital Signal Processors – Architecture, Programming and Applications,, B.Venkataramani, M. Bhaskar, TATA McGraw Hill, 2002

Reference (s)

1. SanjitK.Mitra, Digital Signal Processing, Tata Mc Graw Hill publishers, 3rd Edition, 2009.
2. Alan V. Oppenheim, Ronald W. Schafer Digital Signal Processing, PHI, 4th Edition, 2007
3. Andreas Antoniou, Digital Signal Processing, TATA McGraw Hill , 2006
4. MH Hayes, Digital Signal Processing, Schaum's Outlines, Tata Mc-Graw Hill, 2007

21ECC12 ASIC Verification using System Verilog

3 0 2 4

Course Outcomes

1. Interpret the verification guidelines and data types
2. Execute the programs using assertions and Routines.
3. Demonstrate the System Verilog constructs through simulations
4. Explain the basic OOPs concepts.
5. Organize the design modules in SV test bench.
6. Exemplify the ASIC verification using SV testbench

COs – POs Mapping

COs	PO1	PO2	PO3	PO4	PO5	PSO1
1	2	2	1	2	3	2
2	3	2	2	2	3	3
3	3	2	2	2	3	3
4	2	2	1	2	3	2
5	3	2	2	2	3	3
6	3	2	2	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Verification and Data Types

Introduction to the functional verification Process, The Verification Methodology, Basic Test-bench Functionality, Directed Testing, Constrained-Random Stimulus, Functional Coverage, code coverage, Test-bench Components, Layered Test-bench, Simulation Environment Phases.

Introduction to data types, Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Array Methods, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings, Net Types, Time Scale.

String methods, operators

Practical Components

1. Develop an SV module to demonstrate the declaration of variables
2. Develop a system Verilog code to demonstrate the declaration & application of packed and unpacked arrays.
3. Develop an SV module to demonstrate the application of Ques and simulate
4. Develop a System Verilog program to create two dynamic arrays, insert an elements and display the size.

13+8 Hours

Unit II

Assertions and Routines

Introduction, Assertions: Immediate assertions, Concurrent assertions, Example programs for assertions, Tasks, Functions, Void Functions, Automatic functions, Routine Arguments, Time Scale, System tasks.

Enumerated types, repeat and forever

Practical Components

1. Develop a system Verilog code to demonstrate Immediate assertions
2. Develop a System Verilog testbench to demonstrate the Concurrent assertions
3. Develop a System Verilog test bench to differentiate the calling of a task and a function
4. Develop a System Verilog test bench to demonstrate the passing arguments by value & by reference to a function

11+8 Hours

Unit III

Basic OOPs

Introduction, OOP Terminology, Creating New Objects, Object Deallocation, Using Objects, Static Variables vs. Global Variables, Class Routines, Defining Routines Outside of the Class, Scoping Rules, Using One Class Inside Another, Understanding Dynamic Objects, Copying Objects.

Nested–Inner Class & Anonymous Classes–Generic Class Types

Practical Components

1. Develop an SV module to demonstrate the declaration of objects and classes
2. Write a System Verilog code to demonstrate the derived class to refer to members of the parent class.
3. Develop an SV module to demonstrate the inheritance
4. Develop an SV module to demonstrate the shallow copy to generate the different instances of a class

12+8 Hours

Unit IV

Connecting the Test bench and Design

Introduction to Universal verification methodologies (UVM), Interface: connecting the interface with DUT, Interface parametrization, Interface Driving and Sampling, Case study of Layered testbench: A testbench composed with transaction object, Generator, Driver, Monitor, Scoreboard, Environment, Test case, Interface. EDA tools for the design verification.

Inter process communication: semaphore, mailboxes and event

Practical Components

1. Write a System Verilog program to demonstrate interface
2. Develop a test bench in SV to test a Sequence detector and simulate
3. Develop an SV module to demonstrate the verification of a simple adder using a layered testbench
4. Explore an EDA Development Environment

12+8 Hours

Total: 48+32 Hours

Textbook (s)

1. Chris Spear, “System Verilog for Verification: A Guide to Learning the Test bench Language Features”, Springer-Verlag New York, Inc. Secaucus, NJ, USA, 2006

2. Donald Thomas, "Logic Design and Verification Using System Verilog", Create Space Independent Publishing Platform, 2014.

Reference (s)

1. Language Reference Manual for System Verilog

21ECC22 Embedded System Design and IoT

3 0 2 4

Course Outcomes

1. Implement the interfacing of Input devices with embedded target boards and develop the software for it's operation
2. Implement the interfacing of output devices with embedded target boards and develop the software for it's operation
3. Demonstrate the interfacing of actuators with embedded target boards and develop the software for it's operation
4. Carry-out the interfacing of sensors with embedded target boards
5. Assess real world parameters for IoT applications
6. Demonstrate the configuration of cloud for IoT applications

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5	PSO_1
1	2	-	-	-	-	2
2	3	2	2	2	3	3
3	3	2	2	2	3	3
4	2	-	-	-	-	2
5	3	2	2	2	3	3
6	3	2	2	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Embedded Systems

Definition, Embedded system versus general Computing Systems, Quality Attributes of Embedded Systems, The typical Embedded System, core of Embedded System, Memory, sensors and actuators, Communication Interface, Embedded Firmware, other system components, On board and off board communication interfaces: *UART,* I2C, SPI, BLUE TOOTH, WIFI. Embedded target boards: Arduino board, Raspberry pi. *ZIGBEE, USB*

Practical Components

1. Blinking of LED using embedded target board.
2. Traffic system Controller
3. Interfacing of seven-segment display with embedded target board.

12+6 Hours

Unit II

Hardware and firmware development

Embedded firmware design approaches and development languages, Embedded C, Fundamental Issues in Hardware and Software Co-Design, Hardware software tradeoffs, Integration of Hardware and Firmware. CAD and hardware Translation tools. Pre-processors, Interpreters, Compilers, Linkers. Debugging tools, Simulators and Laboratory tools. *Emulator, beagle bone embedded target board*

Practical Components

1. Interfacing of dc motor with embedded target board and controlling it's speed using PWM concept.
2. Interfacing of LCD with embedded target board.
3. Interfacing of keypad with embedded target board.
4. Interfacing of high voltage device using relay with embedded target board.

12+8 Hours

Unit III

IoT Architecture and Data Analytics

IoT characteristics and Applications, M2M vs. IOT, M2M Value Chains, IoT Value Chains, The international driven global value chain and global information monopolies. Functional View, Information View, Deployment and Operational View, Other Relevant architectural views, sensing the real world for IoT

applications, temperature sensor, humidity and temperature sensor, light dependent register, touch sensor, smoke detector, rain detector, ultrasonic sensor, soil moisture sensor.
LoRa Wan and 6lowpan

Practical Components

1. Interfacing of light dependent register with embedded target board.
2. Interfacing of touch sensor with embedded target board.
3. Interfacing of smoke detector with embedded target board.
4. Interfacing of rain detector with embedded target board.
5. Interfacing of ultrasonic sensor with embedded target board.

12+10 Hours

Unit IV

IoT web Services and business Applications

Introduction to ESP8266 Wi-Fi module, Node MCU Development board, various Wi-Fi library, web server-introduction, installation, configuration, posting sensor(s) data to web server, cloud platforms for IOT, virtualization concepts and cloud architecture, cloud computing, benefits, cloud services - SaaS, PaaS, IaaS, cloud providers & offerings, study of IOT cloud platforms, thing speak API and MQTT, IoT Application : city automation, automotive applications, home automation, process monitoring / automation, smart transportation, smart metering, smart waste management system.
IoT for smart grid, smart healthcare

Practical Components

1. Configure Thingspeak cloud platform for displaying real-time temperature.
2. Configure Blynk cloud platform for turning on/off.
3. Interfacing of humidity and temperature sensor (DHT11) with embedded target board.
4. Interfacing of temperature sensor (LM35) with embedded target board.

12+08 Hours

Total: 48+32 Hours

Textbook (s)

1. Shibu .K.V, Introduction to Embedded Systems, 1st Ed, Tata McGraw Hill Education Private Limited, 2009.
2. Yogesh Misra, Programming and Interfacing with Arduino, CRC Press, 1st Edition, 2021
3. Daniel Minoli, Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David
4. Rajkamal, Internet of things: Architecture and design principles, TMH Publication, 2017

Reference (s)

1. Tammy Noergaard , Embedded systems Architecture, Elsevier publications, 2005
2. Michael Margolis, “Arduino Cookbook”, First Edition, March 2011, O'Reilly Media, Inc
3. Boyle, From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence, 1st Edition, Academic Press, 2014.2M Communications, ISBN: 978-1-118-47347-4, Willy Publications, 2014

21ECC32 Image Processing

3 0 2 4

Course Outcomes

1. Demonstrate the Basic image Operations and fundamental concepts
2. Execute various conversion operations on digital images
3. Implement image enhancement techniques in spatial and frequency domain
4. Implement various filters for image restoration
5. Execute segmentation techniques for digital images
6. Implement image lossless and lossy compression techniques

COs – POs Mapping

COs	PO_1	PO_2	PO_4	PO_5	PSO_2
1	2	-	2	2	2
2	3	2	2	3	3

3	3	2	2	3	3
4	3	2	2	3	3
5	3	2	2	3	3
6	3	2	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Digital Image Fundamentals

Fundamental steps in digital image processing, Elements of visual perception, Image sampling and quantization, Basic relationships between pixels, Image types and formats: Binary image, Gray image, Color image, Color fundamentals, Color models: RGB, HSI and CMY.

Pseudo color Image Processing, Full Color Image Processing

Practical Components

1. Perform basic image operations viz., image read and write on binary image, gray image and color image.
2. Convert a color image to gray image and binary image.
3. Convert color image from RGB model to HSI and HSI to RGB.
4. Perform Image comparison using subtraction

12+8 Hours

Unit II

Image Enhancement

Enhancement in spatial domain: Histogram Processing, Smoothing, Sharpening,

Image transforms and its properties: 2D Discrete Fourier Transform, Discrete Cosine Transform, Discrete Wavelet Transform, Enhancement in Frequency Domain: Smoothing and Sharpening Filters.

Walsh Transform, Haar Transform

Practical Components

1. Carry out intensity transformations on image
2. Perform histogram equalization on digital image
3. Implement image smoothing/sharpening in spatial domain
4. Perform image smoothing/sharpening in frequency domain

12+8 Hours

Unit III

Image Restoration

Image Restoration model, Noise models, Restoration using spatial filtering, Periodic noise reduction by frequency domain filtering, Linear Position-Invariant Degradations, Inverse filtering, Minimum Mean Square Error Filtering, Constrained Least squares filtering.

Estimating the degradation function, Geometric Mean filter

Practical Components

1. Perform image restoration in spatial domain using restoration filters
2. Construct filters to remove various noise effects on the image (Uniform, Gaussian, Poisson, Salt & pepper)
3. Carry out frequency domain filtering for image restoration
4. Perform restoration using Inverse filtering

` **12+8 Hours**

Unit IV

Image Segmentation and Compression

Image segmentation: Fundamentals, Point, Line and Edge detection, Thresholding, Region based Segmentation,

Image Compression: Fundamentals, Image Compression Models, Lossless Compression: Huffman, Arithmetic, Run Length Encoding, Lossy Compression: Transform coding.

Watershed algorithm, JPEG compression standard

Practical Components

1. Implement Prewitt and Sobel operators on an image for edge detection
2. Perform image segmentation based on thresholding
3. Implement Huffman coding technique
4. Implement transform coding technique

12+8 Hours

Total: 48+32 Hours

Textbook (s)

1. Rafel C. Gonzalez and Richard E. Woods, Digital Image Processing, Pearson Education, 3rdEdition 2011
2. S. Sridhar, Digital Image Processing, Oxford publishers, 2nd Edition, 2016
3. Rafel C. Gonzalez and Richard E. Woods, Digital Image Processing using MATLAB, Gatesmark Publishing, 3rdEdition 2020

Reference (s)

1. S. Jayaraman, S. Esakirajan, T. Veerakaumar, Digital Image Processing, McGraw Hill publishers, 2011
2. Anil K. Jain, Fundamentals of Digital Image Processing, Pearson Education, 1st Edition, 2015
3. M. Sonka, V. Hlavac, R. Boyle, Image Processing, Analysis and Machine Vision, Vikas Publishing House, 2001

21EC603 Digital Signal Processing Lab

0 0 3 1.5

Course Outcomes

1. Demonstrate various DSP operations
2. Compute linear and circular convolution between two signals
3. Implement IIR and FIR filter design techniques
4. Execute various multirate signal processing techniques
5. Compute DFT and FFT of discrete time signals
6. Implement the concept of impulse response and multiple frequencies generation of the discrete time system

COs	PO_1	PO_2	PO_4	PO_5	PSO_2
1	2	-	2	3	2
2	3	2	2	3	3
3	3	2	2	3	3
4	3	2	2	3	3
5	3	2	2	3	3
6	3	3	2	3	3

List of Experiments
Students will perform minimum twelve Experiments
Implement the following using MATLAB

1. Generation of Discrete time signals and sum of sinusoidal signals
2. Determination of power and power spectral density of the given sequence
3. Verification of Linear convolution of two given sequences with different lengths.
4. Verification of circular convolution of two given sequences with different lengths.
5. To find frequency response of a given system(transfer function/ difference equation)
6. To find DFT / IDFT of given DT signal.
7. Determination of FFT for a given sequence.
8. Implementation of LP IIR filters for a given sequence.
9. Implementation of HP IIR filters for a given sequence.
10. Implementation of LP FIR filters for a given sequence.
11. Implementation of HP FIR filters for a given sequence.
12. Implementation of Decimation Process
13. Implementation of Interpolation Process
14. Implementation of I/D sampling rate converter
15. Generation of DTMF signals.
16. Impulse Response of First Order and Second Order Systems.

Implement the following using TMS processor

17. To study the architecture of DSP chips – TMS 320C 6X Instructions
18. linear convolution of two given sequences and plot

19. Perform MAC operation using various addressing modes
20. Generation of various signals and random noise
21. Magnitude response FIR LP filter using rectangular windowing technique
22. Magnitude response IIR LP filter

List of Augmented Experiments[1]

1. Mixing and separation of two voice signals
2. Add noise above 3kHz and then remove the Interference for Audio signal
3. Design a notch filter for the removal of power line interference from ECG signal by using TMS processor

Reading Material(s)

1. Digital Signal Processing by Sanjit K.Mitra 2nd Edition , TATA McGraw Hill
2. Digital Signal Processing, Principles, Algorithms, and Applications: John G. Proakis, Dimitris G. Manolakis, Pearson Education / PHI, 2007.
3. Digital signal processing lab Manual

21MPX01 Mini Project

0 0 3 1.5

Course Outcomes

1. Identify a contemporary engineering application to serve the society at large
2. Use engineering concepts and computational tools to get the desired solution
3. Justify the assembled/fabricated/developed products intended
4. Organize documents and present the project report articulating the applications of the concepts and ideas coherently
5. Demonstrate ethical and professional attributes during the project implementation
6. Execute the project in a collaborative environment

COs – POs Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
1	3	2				3	2						3	3
2	3	3			3								3	3
3	3	3	3	2							3		3	3
4										3		3	3	3
5								3					3	3
6									3				3	3

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

21ESX02 Employability Skills II

0 0 2 2

Course Outcomes

1. Demonstrate oral communication and writing skills as an individual to present ideas coherently
2. Develop life skills with behavioral etiquettes and personal grooming.
3. Assess analytical and aptitude skills.
4. Develop algorithms for engineering applications.
5. Solve engineering problems using software.
6. Utilize simulation tools for testing.

COs – POs Mapping

COs	PO1	PO2	PO5	PO8	PO10	PO12
1					3	3
2				1	2	3
3	2	1		2		
4	2		2			
5	2		2			
6	2		2			

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

1. Communication Skills, Confidence and Quantitative Aptitude

Resume (Recap): Resume? Templates? Mistakes to be avoided in a Resume and Steps to be followed in preparing it.

Group Discussions (Recap) & Practice: GD? Stages of a GD, Skills assessed in a GD, Blunders to be avoided, How to excel in a GD?

Practice sessions and sharing Feedback. (Screening sample Videos)

Interview Skills: Interview? Types of Interview, Dos & Don'ts, Skills assessed in an Interview, Mistakes to be avoided, How to equip oneself to excel? How to handle the Typical Interview Questions? (with Examples)

Mock Interviews: Practice sessions with Feedback.

Exercises related to Communication: Email Writing, Voice Versant., etc.

7Hours

2. Quantitative Aptitude

Time and Distance, Problems on Trains, Blood relations, Ratio and Proportions, Calendars, Clocks

8 Hours

Unit II

Verilog constructs for building the testbench

Procedural, Continuous and Procedural continuous assignments, Verilog parameters, inter assignment delay, intra assignment delay, Stem tasks: display tasks, tasks for file operation; Combinational UDPs and Sequential UDPs

Practical Components

1. Perform the simulation of a Verilog testbench to demonstrate the Procedural continuous assignments.
2. Perform the simulation of a Verilog testbench to demonstrate the Verilog parameters.
3. Perform the simulation of a Verilog testbench to demonstrate the inter assignment delay
4. Perform the simulation of a Verilog testbench to demonstrate the inter assignment delay
5. Develop a Verilog testbench that displays the content of a given file
6. Develop a Verilog testbench that writes the content into the file
7. Develop a Verilog testbench to display the file content and detect the end of a given file
8. Perform the simulation of a Verilog testbench to demonstrate the combinational UDP.
9. Perform the simulation of a Verilog testbench to demonstrate the sequential UDP

15 Hours
Total Hours 30

Textbook (s)

2. Padmanabhan, Tattamangalam R., and B. Bala Tripura Sundari. Design Through Verilog HDL. John Wiley & Sons, 2003.

Reference (s)

3. Palnitkar, Samir. *Verilog HDL: a guide to digital design and synthesis*. Vol. 1. Prentice Hall Professional, 2003.
4. Ciletti, Michael D. *Advanced digital design with the Verilog HDL*. Vol. 1. Upper Saddle River: Prentice hall, 2003.

21HSX12 CC & EC Activities II

0 0 1 1

Course Outcomes

1. Interpret and present the abstractive technical information through an activity
2. Think critically in providing solutions to the generic and common problems
3. Demonstrate the creative thinking in dealing with liberal arts
4. Instill team sprit through active engagement with the peer
5. Develop programs of common interest having social impact
6. Empower the under privileged through motivational activities

COs – POs Mapping

COs	PO6	PO7	PO9	PO10
1	-	-	-	3
2	3	2	-	-
3	3	-	-	-
4	-	-	3	-
5	3	-	-	-
6	3	-	-	-

20BEA01 Environmental Studies

0 0 0 0

Course Outcomes:

1. Translate the learner's attitude to think globally and act locally
2. Motivate environmental organizations to create a concern about our present state of Environment.
3. Find solutions for conservation of natural resources
4. Identify the benefits of ecosystem conservation, biodiversity protection, implement pollution prevention and control measures
5. Illustrate social issues of environmental protection and adopt sustainable developmental practices
6. Perceives the basic structure of environmental policy and law pertaining to specific environmental issues (water quality, air quality, biodiversity protection, Forest, etc.)

COs – POs Mapping

COs	PO_1	PO_6	PO_7	PO_{12}
1	1	2	3	1
2	2	-	3	2
3	3	3	-	2
4	-	2	3	2
5	-	-	3	1
6	-	3	2	1

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Multidisciplinary Nature of Environmental Studies & Natural Resources

Definition, Scope and Importance, Multidisciplinary nature of Environmental Studies, Value of Nature - Productive, Aesthetic/Recreation, Option, Need for Public Awareness, Institutions (BNHS, BVIEER, ZSI, BSI) and People in Environment (Medha Patkar, Sundarlal Bahuguna, Indira Gandhi, Rachael Carson).

Natural Resources: Renewable and Non-renewable resources – Importance, uses, overexploitation/threats, and conservation of (i) forest (ii) water (iii) mineral (iv)food and (v) energy resources. (The topics include benefits and problems associated with dams, mining and case studies), role of an individual in conservation of natural resources.

Unit II

Ecosystem & Biodiversity

Ecosystems: Concept of an ecosystem, Structure and function of an ecosystem, Biogeological cycles (Energy flow, Carbon and Nitrogen Cycles), Ecological succession, Food chains, food webs and ecological pyramids. Introduction, types, characteristic features, structures and functions of the following ecosystems: a. Forest Ecosystem b. Aquatic Ecosystem

Biodiversity and its Conservation: Definition and levels of biodiversity, Bio-geographical classification of India, hot spots of biodiversity - India as a mega diversity nation, Threats to biodiversity, Endangered and endemic species of India, Conservation of biodiversity: In-situ and Ex-situ conservation.

Unit III

Environmental Pollution & Social Issues

Environmental Pollution: Definition, Cause, effects, control measures and case studies of: Air pollution b. Water pollution c. Soil pollution

Solid waste Management: Causes, effects and control measures of urban and industrial wastes. Disaster management (floods and cyclones)

Social Issues and the Environment: Sustainability, Urban problems related to energy, Water conservation and watershed management, Resettlement and rehabilitation of people; Environmental ethics: Issues and possible solutions, global warming, ozone layer depletion, Consumerism and waste products

Unit IV

Human Population and the Environmental Acts

Human Population and the Environment: Population growth, Affluence, Technology and Environmental Impact (Master Equation), Population explosion and Family Welfare Programme, Value Education, HIV/AIDS, Women and Child Welfare, Role of information Technology in Environment and human health.

Environment Protection Acts: Air (Prevention and Control of Pollution) Act, Water (Prevention and control of Pollution) Act, Wildlife Protection Act and Forest Conservation Act. Issues involved in enforcement of environmental legislation.

Text Book(s) and Reading Material (s)

1. T. E. Graedel, B. R. Allenby, Industrial Ecology and Sustainable Engineering, 1st Edition, Pearson Publications, 2009.
2. W. P. Cunningham, M.A. Cunningham, Principles of Environmental Science, 6th Edition, Tata McGraw Hill, 2008.
3. A. Kaushik, C. P. Kaushik, Perspectives in Environmental Studies, 4th Edition, New Age International Publishers, 2008.
4. T. E. Graedel, B. R. Allenby, Industrial Ecology and Sustainable Engineering, 1st Edition, Pearson Publications, 2009.
5. E. Bharucha, Textbook of Environmental Studies, 1st Edition, University Press (India) Pvt. Ltd., 2005.
6. H. S. Peavy, D. R. Rowe, G. Tchobanoglous, Environmental Engineering, 1st Edition, McGraw Hill Int. ed., 1984.
7. http://172.30.1.222/wbc/it/schedule.aspx.
8. http://172.30.1.8/wbc/it/coursepage.aspx.
9. https://www.edx.org/course/environmental-protection-and-sustainability.

21ECC13 Analog and Mixed Signal VLSI Design

3 0 0 3

Course Outcomes

1. Illustrate the MOS device models Single-stage amplifiers and Current mirrors
2. Explain the operation of Differential amplifiers
3. Demonstrate the operation of Op-amp internal circuits
4. Demonstrate the operation of switched capacitor circuits
5. Demonstrate the operation of continuous and discrete-time filters
6. Outline the operation of data conversion circuits

COs – POs Mapping

COs	PO1	PO2	PO3	PO4	PSO1
1	2	-	-		2
2	2	-	-		2
3	3	2	2		3
4	3	2	2	2	3
5	3	2	2	2	3
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Basic Analog Circuits

Introduction analog design, MOS device capacitances, MOS Small-signal model, Second order effects, CS amplifier with resistive load, CS stage with current source load, CS stage with source degeneration, Cascode stage, Current Mirrors: Basic current mirrors, small-signal analysis of a simple current source, Common source amplifier with current mirror as a load, Cascode current mirrors

Advanced MOS Modelling, Single Stage Amplifiers

12 Hours

Unit II

Differential amplifiers and Op-amp circuit

Differential amplifiers: single-ended and differential amplifier operation, basic differential pair, differential pair with MOS loads, differential pair with current source load, Operational Amplifiers: One stage Op-Amp: Simple Op-Amp topologies, Cascode Op-Amp, Folded cascode op-amp, Two-stage Op-Amp, comparison of op-amp topologies, slew-rate

Common Mode Feedback, Power supply rejection

12 Hours

Unit III

Switched capacitors and filters

Switched capacitors: Introduction to the switched capacitor circuits, non-idealities in switched-capacitor circuits, Basic building blocks, Basic Operation and Analysis, parasitic sensitive integrator, parasitic insensitive integrator, Filters: First order filters, biquad filters, charge injection, switch sharing, switched capacitor gain circuits

Switched-capacitor filter applications, Stability of Discrete-Time Filters

12 Hours

Unit IV

Data converters

Data Converter Fundamentals: Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Signed Codes; Nyquist-Rate Digital to Analog converters: Decoder-Based, Binary-Scaled, Hybrid DACs; Nyquist-Rate Analog to Digital converters: Algorithmic, Two-step, Folding ADCs; Bandgap reference

Time-interleaved A/D converters, PTAT, CTAT

12 Hours

Total: 48 Hours

Textbook (s)

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2nd Edition, McGraw-Hill, 2017
2. Tony Chan Carusone, David Johns, Kenneth Martin: Analog Integrated Circuit Design, 2nd Edition, John Wiley Publications, 2011
3. R. Jacob Baker, CMOS mixed-signal circuit design, Wiley India, IEEE press, reprint 2008
4. Rudy V. dePlassche, CMOS Integrated ADCs and DACs, Springer, Indian edition, 2005

Reference (s)

1. Philip E. Allen & Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, 2002
2. M. Burns et al., An introduction to mixed-signal IC test and measurement by, Oxford university press, first Indian edition, 2008
3. R. Jacob Baker, CMOS circuit design, layout and simulation, Revised second edition, IEEE press, 2008
4. Arthur B. Williams, Electronic Filter Design Handbook, McGraw-Hill, 1981
5. R. Schauman, Design of analog filters, Prentice-Hall, 1990
6. Ramakant A. Gayakwad, Op-Amps and Linear Integrated Circuits, Fourth edition, Pearson Education, 2015

21ECC23 Real Time Operating Systems

3 0 0 3

Course Outcomes

1. Summarize the real time systems and its characteristics
2. Exemplify classification and modelling of time constraints
3. Assess the Task synchronisation in Real Time Operating System
4. Illustrate real time communication and its applications
5. Compare various Real Time Scheduling Approaches
6. Outline the suitable real time operating systems for commercial applications

COs – POs Mapping

COs	PO1	PO2	PO_3	PO_4	PSO1
1	2				2
2	2				2
3	3	2	2		3
4	2			2	2
5	3	2	2	2	3
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Real Time System

Introduction to real time system, applications of a real time system, characteristics of real time systems, safety and reliability, Types of real time tasks – Hard real time task, Soft real time task and Firm real time task , timing constraints, classification of timing constraints – delay constraint, deadline constraint and duration constraint, modeling timing constraints.

fault Tolerant Applications, classification of systems on the basis of real time task

12 Hours

Unit II

Real Time Operating System

Operating system Basics, features of General Purpose Operating System (GPOS), features of Real Time Operating System (RTOS), Process, Threads and Tasks, multiprocessing and multitasking, types of multitasking, Task synchronisation – Racing and Deadlock. Task synchronisation techniques – Mutual Exclusion through busy waiting/spin lock, Mutual Exclusion through sleep & Wakeup, selection criteria for an RTOS

Identify some RTOS for review, Embedded Programming in C

12Hours

Unit III

Real Time Scheduling Approaches

Task scheduling, Non-Preemptive Scheduling – First-Come-First-Served (FCFS) scheduling, Last-Come-First-Served (LCFS) scheduling, Shortest Job First (SJF) scheduling, Priority Based scheduling. Preemptive

Scheduling – Preemptive Shortest Job First (SJF) scheduling/Shortest Remaining Time (SRT), Round Robin (RR) Scheduling. Rate monotonic algorithm (RMA)
Rate Monotonic Algorithm, Hybrid scheduler

13 Hours

Unit IV
Commercial Real Time Operating Systems

Unix as a real time operating system, Windows as a real time operating system, POSIX

Real time Communication - Basic concepts, Real-time communication in a LAN and Real-time communication over packet switched networks, applications requiring real time communication
µC/OS-II, VxWorks

11 Hours
Total: 48 Hours

Textbook (s)

1. Rajib Mall, Real-time Systems Theory and Practice, 1st edition, Pearson Publication, 2008
2. Shibu .K.V, Introduction to Embedded Systems, 1st Ed, Tata McGraw Hill Education Private Limited, 2009.

Reference (s)

1. Jane W. S. Liu, Real-Time Systems, Pearson Education, 2000.
2. C.M. Krishna and K.G. Shin, Real-Time Systems, TMH, 2009.

21ECC33 Multimedia Communications

3 0 0 3

Course Outcomes

1. Summarise basics of different multimedia networks and applications.
2. Demonstrate compression techniques of text and audio.
3. Assess video compression techniques.
4. Illustrate different multimedia information networks.
5. Demonstrate enterprise networks and Internet.
6. Justify the real-time entertainment networks and high speed modems.

COs – POs Mapping

COs	PO1	PO2	PO_3	PO_4	PSO2
1	2				2
2	2				2
3	3	2	2		3
4	2			2	2
5	3	2	2	2	3
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I
Introduction
Introduction, Multimedia information representation, multimedia networks, multimedia applications, Networking terminology, Digitization principles, Text, Images, Audio and Video.
Application QoS, Video content

12 Hours

Unit II
Data Compression
Introduction, Compression principles, Text compression techniques, Image Compression techniques, Audio compression techniques, Video compression techniques.
JPEG Decoding, Reversible VLCs

12 Hours

Unit III

Multimedia Information Networks

Introduction, LANs, Ethernet/IEEE802.3, Token ring, Bridges, FDDI, High-speed LANs, LAN protocol, IP Datagrams, Fragmentation, IP Address, ARP and RARP, Routing algorithms, ICMP, Support, IPv6.
Multisite LAN Interconnection technologies, QoS Support

12 Hours

Unit IV

Networks and Modems: Introduction, Cell format, Switch and Protocol Architecture ATM LANs, Cable TV Networks, Satellite Television Networks, Terrestrial television networks, ISDN, DSL and Cable Modems
ATM MANs, High Speed PSTN Access Technologies.

12 Hours
Total: 48 Hours

Textbook (s)

1. Fred Halsall, Multimedia Communication, Pearson education, 2001.
2. K. R. Rao, Zoran S. Bojkovic and Dragorad A. Milovanovic, Multimedia Communication Systems, Pearson education, 2004.

Reference (s)

1. Ralf Steinmetz, Klara Nahrstedt, Multimedia: Computing, Communications and Applications, Pearson education, 2004.
2. John Billamil, Louis Molina, Multimedia: An Introduction, PHI, 2002.
3. Nalin K. Sharda, Multimedia Information Networking, PHI, 2003.
4. Prabhat K. Andleigh, Kiran Thakrar, Multimedia Systems Design, PHI, 2004.

21EC009 UHF and EHF communication systems

3 0 0 3

Course Outcomes

1. Interpret the various subsystems and their parameters
2. Asses various multiple access techniques and spread spectrum techniques
3. Demonstrate the concepts of Link Design
4. Explain RADAR parameters and applications
5. Demonstrate the operation of CW and MTI RADARs
6. Differentiate the tracking techniques for RADARs

COs – POs Mapping

COs	PO1	PO 2	PO3	PO4	PSO2
1	2	-			2
2	3	2	2		3
3	3	2	2		3
4	2	-		2	2
5	3	2		2	3
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction to Satellite and Subsystems

Introduction to spectrum characteristics and Spectrum ranges, basic Concepts of Satellite Communications, Applications, Orbital Mechanics, Orbit determination, Look Angle determination, Orbital perturbations, launches and launch vehicles, Orbital effects in communication systems performance. Attitude and orbit control system, telemetry, tracking, Command and monitoring, power

systems, communication subsystems, Satellite antennas.
Orbit Determination, Manned Space Vehicles

12 Hours

Unit II

Satellite Link Design and Multiple Access Techniques

Satellite link Design: Basic transmission theory, system noise temperature and G/T ratio.
Multiple Access Techniques: Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA), Demand Assignment Multiple Access (DAMA) , Code Division Multiple Access (CDMA), Spread spectrum techniques
Design of UP & Down links, Packet radio systems and Protocols

12 Hours

Unit III

Basics of Radar

Introduction, Maximum Unambiguous Range, Radar Block Diagram and Operation, Simple form of Radar Equation, Radar Cross Section of simple Targets, PRF and Range Ambiguities. CW and Frequency Modulated Radar: Doppler Effect, CW Radar-Block Diagram, MTI and Pulse Doppler Radar**:** Introduction, Principle, Delay Line Cancellers, Filter Characteristics, Blind Speeds, Double Cancellation, Staggered PRFs, Range Gated Doppler Filters, MTI versus Pulse Doppler Radar.

Multiple Frequency CW Radar, MTI Radar with Power Oscillator Transmitter **13 Hours**

Unit IV

Tracking Radar

Tracking with Radar, Sequential Lobing, Conical Scan, Amplitude Comparison monopulse radar using one coordinate system and Phase Comparison methods, Target Reflection Characteristics and Angular Accuracy, Tracking in Range, Acquisition and Scanning Patterns, Comparison of Trackers, Radomes, Frequency scan Arrays, Radar Display types, Branch type and Balanced type duplexers
Amplitude Comparison using two coordinate system, Circulators as Duplexers

11 Hours
Total: 48 Hours

Textbook (s)

1. Timothy Pratt, Charles Bostian and Jeremy Allnutt, WSE, Satellite Communications, Wiley Publications, 2nd Edition, 2004
2. Wilbur L. Pritchard, Robert A Nelson and Henri G.Suyderhoud, Satellite Communications Engineering, 2nd Edition, Pearson Publications, 2012
3. Merrill I. Skolnik Introduction to Radar Systems, Tata McGraw-Hill, Third Edition, 2001

Reference (s)

1. K.N. Raja Rao, Fundamentals of Satellite Communications, PHI, 2004
2. Dennis Roddy , Satellite Communications, McGraw Hill, 2nd Edition, 1996
3. Gottapu Sasibhushana rao, Microwave & Radar Engineering, Pearson Education, 2013

21PWX01Project Work

0 0 16 8

Course Outcomes

1. Identify a contemporary engineering application to serve the society at large
2. Use engineering concepts and computational tools to get the desired solution
3. Justify the assembled/fabricated/developed products intended
4. Organize documents and present the project report articulating the applications of the concepts and ideas coherently
5. Demonstrate ethical and professional attributes during the project implementation
6. Execute the project in a collaborative environment

COs – POs Mapping

COs	PO1	PO2	PO3	PO4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
1	3	2				3	2						3	3
2	3	3			3								3	3
3	3	3	3	2							3		3	3
4										3		3	3	3
5								3					3	3
6									3				3	3

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

21SIX02 Summer Internship II

0 0 0 1.5

Course Outcomes

1. Demonstrate communication skills to meet the requirement of industry
2. Develop logical thinking and analytical skills to thrive in competitive examinations
3. Use mathematical concepts to solve technical quizzes
4. Develop technical skills to work out real time problems
5. Develop algorithms for different applications
6. Solve industry defined problems using appropriate programming skills

COs – POs Mapping

COs	PO_1	PO_2	PO_5	PO_6	PO_{10}	PO_{12}
1					3	
2	3	1				
3	3					
4	3	1	3			3
5	3	1	3	3		3
6	3	1	3			3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

21EC013 Image Processing for Engineering Applications

0 0 0 3

Course Outcomes:

1. Illustrate the fundamentals of image processing using MATLAB
2. Summarize various Feature extraction techniques.
3. Asses spatial filters for image processing applications
4. Illustrate the concepts of image Registration
5. Illustrate the concepts of image fusion
6. Outline 3D image visualization

COs – POs Mapping

COs	PO_1	PO_2	PO3	PO4	PSO_2
1	2	1			2
2	2	1			2
3	3	2	2		3
4	3	2		2	3
5	2	1		2	2
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

IMAGE PROCESSING WITH MATLAB

What are Digital Images, Working with Image Data, Representing Images in MATLAB, Working with Image Data, Image Display vs. Image Data, Viewing Meta-Data and Images, Grayscale Images, Introduction to Color Spaces, Thresholding color Image, Adjusting Contrast in Grayscale and color Images, Other Approaches to Image Enhancement

12 Hours

Unit II

FEATURE EXTRACTION

First and second order edge detection operators, Phase congruency, Localized feature extraction - detecting image curvature, shape features, Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors Autocorrelation, Co-occurrence features, Runlength features, Fractal model based features, Gabor filter, wavelet features.

12 Hours

Unit III

REGISTRATION AND IMAGE FUSION

Registration - Pre-processing, Feature selection - points, lines, regions and templates Feature correspondence - Point pattern matching, Line matching, Region matching, Template matching. Transformation functions - Similarity transformation and Affine Transformation. Resampling – Nearest Neighbour and Cubic Splines. Image Fusion - Overview of image fusion, pixel fusion, and wavelet based fusion -region based fusion.

12 Hours

Unit IV

3D IMAGE VISUALIZATION

Sources of 3D Data sets, Slicing the Data set, Arbitrary section planes, The use of color, Volumetric display, Stereo Viewing, Ray tracing, Reflection, Surfaces, Multiple connected surfaces, Image processing in 3D, Measurements on 3D images.

12 Hours

Total: 48 Hours

Text Book(s):

1. Ardeshir Goshtasby, " 2D and 3D Image registration for Medical, Remote Sensing and Industrial Applications",John Wiley and Sons,2005.
2. Anil K. Jain, Fundamentals of Digital Image Processing', Pearson Education, Inc., 2002.
3. John C.Russ, "The Image Processing Handbook", CRC Press,2007.

Reference Book(s)

1. Mark Nixon, Alberto Aguado, "Feature Extraction and Image Processing", Academic Press,2008.
2. Rafael C. Gonzalez, Richard E. Woods, Digital Image Processing', Pearson,Education, Inc.,Second Edition, 2004.
3. Rick S.Blum, Zheng Liu, "Multisensor image fusion and its Applications", Taylor& Francis,2006

21FIX01 Full Semester Internship

0 0 0 9

Course Outcomes

1. Use the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems
2. Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences
3. Select appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations
4. Use ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
5. Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings
6. Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions

COs – POs Mapping

COs	PO_1	PO_2	PO_5	PO_8	PO_9	PO_{10}	PSO_1	PSO_2
1	3	-	-	-	-	-	3	3
2	-	3	-	-	-	-	3	3
3	-	-	3	-	-	-	3	3
4	-	-	-	3	-	-	-	-
5	-	-	-	-	3	-	-	-
6	-	-	-	-	-	3	-	-

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Department of Electronics and Communication Engineering

Minimum Credits to be earned: 160 (for Regular Students)

1st SEMESTER

Pattern-I - A to H Sections				**Pattern-II - I to P Sections**			
S. No.	**Course Code**	**Course Name**	**Credits**	**S. No.**	**Course Code**	**Course Name**	**Credits**
1	23PYX01	Engineering Physics	3	1	23CYX01 23CYX02	Chemistry (EEE, ECE, CSE, AIML, AIDS, IT) Engineering Chemistry (CE, ME)	3
2	23MAX01	Linear Algebra& Calculus	3	2	23MAX01	Linear Algebra& Calculus	3
3	23BEX01	Basic Electrical and Electronics Engineering	3	3	23BEX02	Basic Civil & Mechanical Engineering	3
4	23BEX03	Introduction to Programming	3	4	23BEX03	Introduction to Programming	3
5	23BEX04	Engineering Graphics	3	5	23HSX01	Communicative English	2
6	23PYX02	Engineering Physics Lab	1	6	23CYX03 23CYX04	Chemistry Lab (EEE, ECE, CSE, AIML, AIDS, IT) Engineering Chemistry Lab (CE, ME)	1
7	23BEX05	Electrical & Electronics Engineering Workshop	1.5	7	23BEX06	Engineering Workshop	1.5
8	23BEX07	Computer Programming Lab	1.5	8	23BEX07	Computer Programming Lab	1.5
9	23BEX08	IT Workshop	1	9	23HSX02	Communicative English Lab	1
				10	23HSX11	ECA (Yoga / Sports)	0.5
				11	23HSX12	CCA (NSS/NCC/Community Service)	0.5
		Total	**20**			**Total**	**20**

2nd SEMESTER

Pattern-I - A to H Sections				Pattern-II - I to P Sections			
S. No.	**Course Code**	**Course Name**	**Credits**	**S. No.**	**Course Code**	**Course Name**	**Credits**
1	23CYX01 23CYX02	Chemistry (EEE, ECE, CSE, AIML, AIDS, IT) Engineering Chemistry (CE, ME)	3	1	23PYX01	Engineering Physics	3
2	23MAX02	DIFFERENTIAL EQUATIONS AND VECTOR CALCULUS	3	2	23MAX02	DIFFERENTIAL EQUATIONS AND VECTOR CALCULUS	3
3	23BEX02	Basic Civil & Mechanical Engineering	3	3	23BEX01	Basic Electrical and Electronics Engineering	3
4	23ME201 23CS201 23EE201 23EC201 (Branch Specific Theory)	Engineering Mechanics (Civil, Mech) ; Data Structures (CSE, CSE-AI&DS, CSE-AI&ML, IT) ; Electrical Circuit Analysis-1 (EEE); Network Analysis (ECE);	3	4	23ME201 23CS201 23EE201 23EC201 (Branch Specific Theory)	Engineering Mechanics (Civil, Mech) ; Data Structures (CSE, CSE-AI&DS, CSE-AI&ML, IT) ; Electrical Circuit Analysis-1 (EEE); Network Analysis (ECE);	3
5	23HSX01	Communicative English	2	5	23BEX04	Engineering Graphics	3
6	23CYX03 23CYX04	Chemistry Lab (EEE, ECE, CSE, AIML, AIDS, IT) Engineering Chemistry Lab (CE, ME)	1	6	23PYX02	Engineering Physics Lab	1
7	23BEX06	Engineering Workshop	1.5	7	23BEX05	Electrical & Electronics Engineering Workshop	1.5
8	23CE201 23CS202 23EE202 23EC202 23ME202 (Branch Specific Lab)	Engineering Mechanics and Building Practices Lab (Civil); Data Structures Lab (CSE, CSE-AI&DS, CSE-AI&ML, IT); Electrical Circuits Lab (EEE); Network Analysis Lab (ECE); Engineering Mechanics Lab (Mech);	1.5	8	23CE201 23CS202 23EE202 23EC202 23ME202 (Branch Specific Lab)	Engineering Mechanics and Building Practices Lab (Civil); Data Structures Lab (CSE, CSE-AI&DS, CSE-AI&ML, IT); Electrical Circuits Lab(EEE); Network Analysis Lab(ECE); Engineering Mechanics Lab (Mech);	1.5
9	23HSX02	Communicative English Lab	1	9	23BEX08	IT Workshop	1
10	23HSX11	ECA (Yoga / Sports)	0.5				
11	23HSX12	CCA (NSS/NCC/Community Service)	0.5				
		Total	**20**			**Total**	**20**

No	Course Code	Course	POs	Contact Hours			
				L	T	P	C
Third Semester							
1	23MA301	Complex Variables	1, 2,3,PSO2	3	-	-	3
2	23EC301	Electronic Devices and Circuits	1,2,3,PSO1	3	-	-	3
3	23EC302	Python Programming	1,2, 4,5	3	-	2	4
4	23EC303	Logic Circuit Design	1,2, 3,PSO1	3	-	-	3
5	23EC304	Random Variables and Stochastic Processes	1,2,3, PSO2	3	-	-	3
6	23EC305	Signals & Systems	1,2,4,5, PSO2	3	-	2	4
7	23EC306	Electronic Devices and Circuits Lab	1, 2, 4, PSO1	-	-	3	1.5
8	23EC307	Logic Circuit Design Lab	1, 2, 4, 5, PSO1	-	-	3	1.5
9	23ESX01	Employability Skills I	1,2,5,8,10,12	-	-	2	--
		Audit course					--
			Total	**18**	**0**	**13**	**23**
Fourth Semester							
1	23CSE01	Object Oriented Programming	1,2, 3,5	3	-	-	3
2	23EC401	Analog and Digital Communications	1,2, 3,PSO2	3	-	-	3
3	23EC402	Analog Electronic Circuits	1, 2, 4,5, PSO1	3	-	2	4
4	23EC403	Electromagnetic Waves & Transmission Lines	1,2,3, PSO2	3	-	-	3
5	23EC404	Linear Control Systems	1, 2, PSO1, PSO2	3	-	-	3
6	23CSE02	Object Oriented Programming Lab	1,2,4,5	-	-	3	1.5
7	23EC405	Analog and Digital Communications Lab	1, 2, 4,5, PSO2	-	-	3	1.5
8	23ESX01	Employability Skills I	1,2,5,8,10,12	-	-	2	2
			Total	**15**	**0**	**10**	**21**
Fifth Semester							
1	23EC501	Linear and Digital IC Applications	1,2, 3,PSO1	3	-	-	3
2	23EC502	Microprocessors and Microcontrollers	1, 2, 3, 4, 5, PSO1	3	-	2	4
3	23EC503	VLSI Design	1, 2,3, 4, 5, PSO1	3	-	2	4
4	23EC504	Antennas and Microwave Engineering	1,2, 3,PSO2	3	-	-	3
5		Elective I (Professional Elective)		3	-	-	3
6		Elective II (Open Elective I)		3	-	-	3
7	23EC505	Linear IC Applications Lab	1,2,3, 4, PSO1	-	-	3	1.5
8	23TPX01	Term Paper	1,4,9,10,12,PSO1,PSO2	-	-	3	1.5
9	23ESX02	Employability Skills II	1,2,5,8,10,12	-	-	2	--
10	23SIX01	Summer Internship I	1,2,8,10,12	-	-	-	1
			Total	**18**	**0**	**13**	**24**
Sixth Semester							
1	23HSX10	Engineering Economics and Project Management	1,10,11,12	3	-	-	3
2	23EC601	Cellular and Mobile Communications	1,2, 3,PSO2	3	-	-	3
3	23EC602	Digital Signal Processing	1,2, 3,PSO2	3	-	-	3

4		Elective III (Professional Elective)		3	-	2	4
5		Elective IV (Open Elective II)		3	-	-	3
6	23EC603	Digital Signal Processing Lab	1,2,4,5, PSO2	-	-	3	1.5
7	23 MPX01	Mini Project	ALL	-	-	3	1.5
8	23ESX02	Employability Skills II	1,2,5,8,10,12	-	-	2	2
9	23ATX01	Environmental Studies	1,6,7,12	-	-	-	-
10	23ATX02	Human Values and Professional Ethics	----------	-	-	-	-
11	23ATX----	Audit Course	----------	-	-	-	-
			Total	**15**	**0**	**11**	**21**
Seventh Semester							
1	23PWX01	Project Work	ALL	-	-	16	8
2		Elective V (Professional Elective)		3	-	-	3
3		Elective VI (Professional Elective)		3	-	-	3
4		Elective VII (Open Elective III)		3	-	-	3
5	23SIX02	Summer Internship II	1,2,8,10,12	-	-	-	1
			Total	**9**	**0**	**16**	**18**
Eighth Semester							
1	23FIX01	Full Semester Internship (FSI)	1,2,5,8,9,10, PSO1, PSO2	-	-	**-**	8
2		Elective VIII (Professional Elective)		-	-	**-**	3
3		Elective IX (Open Elective IV)		-	-	**-**	2
			Total	**0**	**0**	**-**	**13**

List of Electives

Language Electives							
No.	**Course Code**	**Course**	**POs**	**Contact Hours**			
				L	**T**	**P**	**C**
1	23HSX03	Advanced Communicative English	10,12	2	-	-	2
2	23HSX04	Communicative German		2	-	-	2
3	23HSX05	Communicative French		2	-	-	2
4	23HSX06	Communicative Japanese		2	-	-	2
5	23HSX07	Communicative Spanish		2	-	-	2
6	23HSX08	Communicative Korean		2	-	-	2
7	23HSX09	Communicative Hindi		2	-	-	2
Elective I							
Career Path I, II, III and Other Core Electives							
1	23ECC11	RTL Coding Techniques (Chip Design Career Path)	1, 2, 3, PSO1	3	-	-	3
2	23ECC21	IoT Architecture and Protocols (Embedded System Design Career Path)	1, 2, 3,6,7,8,PSO1,PSO_2	3	-	-	3
3	23ECC31	Coding Theory and Techniques Techniques (Advanced Communications)	1, 2, 3,PSO2	3	-	-	3
4	23IT304	Database Management Systems	1, 2, 3,PSO_2	3	-	-	3
5	23CS303	Data Structures	1, 2,PO_{12}	3	-	-	3
6	23CS403	Computer Organization and Architecture	1,2, PO_{12},PSO_1	3	-	-	3
		MOOCs		-	-	-	3
Elective III							
Career Path I, II, III and Other Core Electives							
1	23ECC12	System Verilog for Verification (Chip Design Career Path)	1, 2, 3,4,5, PSO1	3	-	2	4
2	23ECC22	Embedded System Design and ARM Processor (Embedded System Design Career Path)	1, 2, 3, 4, 5, PSO1	3	-	2	4
3	23ECC32	Principles of MIMO-OFDM Communications (Advanced Communications)	1, 2,4,5, PSO2	3	-	2	4
4	23EC004	Virtual Instrumentation	1, 2, 4, 5, PSO2	3	-	2	4
5	23EC005	Cryptography and Network Security	1, 3, 4, 5, PSO1	3	-	2	4
6	23CS503	Computer Networks	1,2,4,5,PSO1,PSO2	3	-	2	4
		MOOCs		-	-	-	3
Elective V							
Career Path I, II, III and Other Core Electives							
1	23ECC13	VLSI Physical Design with Timing Analysis (Chip Design Career Path)	1, 2, 3, PSO1	3	-	-	3
2	23ECC23	Real Time Operating Systems (Embedded System Design Career Path)	1,2, 3,PSO1	3	-	-	3
3	23ECC33	5G Communications (Advanced Communications)	1, 2, 3,7,PSO2	3	-	-	3
4	23EC006	Wireless Sensor Networks	1, 2, PSO1, PSO2	3	-	-	3
5	23IT403	Operating Systems	1, 12	3	-	-	3
6	23CS603	Software Engineering	4, 5, 8, 11, PSO1	3	-	-	3
		MOOCs		-	-	-	3
Elective VI							

1	23EC007	Design for testability	1, 2, 3, PSO1	3	-	-	3
2	23EC008	Biomedical Signal Processing	1, 2, 3,PSO2	3	-	-	3
3	23EC009	Digital Image Processing	1, 2, 3,PSO2	3	-	-	3
4	23EC010	Neural Networks and Deep Learning	1, 2, PSO1, PSO2	3	-	-	3
		MOOCs		-	-	-	3
Elective VIII (Professional Elective)							
1	23EC012	Real-Time Systems Design and Analysis	1, 2, 3,PSO1	-	-	-	3
2	23EC013	UHF and EHF communication systems	1, 2, 3,PSO2	-	-	-	3
3	23EC014	Computer Architecture	1, 2, 3,PSO1	-	-	-	3
Audit Course							
1	23AT001	Communication Etiquette in Workplaces	-	-	-	-	-
2	23AT002	Contemporary India: Economy, Policy and Society	-	-	-	-	-
3	23AT003	Design The Thinking	-	-	-	-	-
4	23AT004	Ethics and Integrity	-	-	-	-	-
5	23AT005	Indian Heritage and Culture	-	-	-	-	-
6	23AT006	Intellectual Property Rights and Patents	-	-	-	-	-
7	23AT007	Introduction to Journalism	-	-	-	-	-
8	23AT008	Mass Media Communication	-	-	-	-	-
9	23AT009	Science, Technology and Development	-	-	-	-	-
10	23AT010	Social Responsibility	-	-	-	-	-
11	23AT011	The Art of Photography and Film Making	-	-	-	-	-
12	23AT012	Gender Equality for Sustanibity	-	-	-	-	-
13	23AT013	Women in Leadership	-	-	-	-	-
14	23AT014	Introduction to Research Methodology	-	-	-	-	-
15	23AT015	Climate Change and Circular Economy	-	-	-	-	-
B. Tech. (Honors)							
Domain I VLSI Circuit Design and Verification							
01	23ECH11	System on Chip Design	1,2,3,PSO1	4	-	-	4
02	23ECH12	CMOS Logic Circuit Design	1, 2, 3, PSO1	4	-	-	4
03	23ECH13	Low Power VLSI Design	1, 2, 3, PSO1	4	-	-	4
04	23ECH14	VLSI Fabrication Technology	1,2,3, PSO1	4	-	-	4
Domain II Robotics and Automation							
01	23ECH21	Advanced Controllers	1, 2, 3, PSO1	4	-	-	4
02	23ECH22	Robots and Control	1, 2, 3, PSO1	4	-	-	4
03	23ECH23	Industrial Automation	1, 2, PSO1, PSO2	4	-	-	4
04	23ECH24	Distributed Embedded systems	1, 2, 3, PSO1	4	-	-	4
B. Tech. (Minors)							
VLSI Design							
01	23ECM01	Fundamentals of VLSI design		4	-	-	4
02	23ECM02	Digital Design with Verilog		4	-	-	4
03	23ECM03	Verification Using System Verilog		4	-	-	4
04	23ECM04	VLSI Design Flow: RTL to GDS		4	-	-	4

23EC301 Electronic Devices and Circuits

3 0 0 3

Course Outcomes

1. Explain characteristics and applications of semiconductor devices
2. Illustrate the characteristics of transistors
3. Construct different biasing circuits for BJT
4. Illustrate h-parameter representation and Hybrid-model of transistor
5. Analyse low frequency and high frequency single stage amplifiers
6. Construct multi stage amplifiers

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_1
1	2				2
2	2				2
3	3	2	2		3
4	2			2	2
5	3	2	2	2	3
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Semiconductors–Diodes

Construction and characteristics- PN Junction diode, Zener diode, Tunnel diode, Photo diode, light emitting diode, UJT and SCR, Transition and Diffusion Capacitance of PN junction diode. Rectifiers - Half wave rectifier, Full wave center Tapped rectifier, Bridge rectifier, overview of filters, Regulator using Zener diode.

Diode current equation, Diode Junction Breakdowns mechanisms

12 Hours

Unit II

BJT & FET

Bipolar Junction transistors - Transistor current components, Transistor as an amplifier, Input and Output characteristics of Common Base and Common Emitter configurations , BJT biasing - Criteria for fixing operating point, Self-bias, Thermal run away, Thermal stability, Characteristics of JFET, MOSFET characteristics- Enhancement mode and depletion mode.

Stabilization techniques, Compensation techniques

12 Hours

Unit III

Low Frequency Amplifiers

h-parameter representation of a transistor, Analysis of single stage transistor amplifier using h-parameters - Voltage gain, Current gain, Input impedance and Output impedance of CE, CB, and CC amplifiers using exact and approximate analysis. Analysis of single stage FET amplifiers - voltage gain, input impedance and output impedance of CS, CG, and CD amplifiers.

Buffer amplifier, MOSFET Amplifier

12 Hours

Unit IV

High Frequency and Multi Stage Amplifiers

Hybrid -CE transistor Model, Determination of Hybrid -Conductances, Miller's and Dual of Miller's theorem, CE Short Circuit Current gain, Parameters of f_β and f_T , Frequency response of RC coupled CE amplifiers. n–Stage Cascaded Amplifier, Darlington pair, Cascode amplifier, CE-CC Amplifiers.

Transformer coupled amplifier, CE current gain with load

12 Hours

Total: 48 Hours

Textbook (s)

1. J.Millman, C.C.Halkias and Chetan D Parikh, Integrated Electronics, 2nd Edition, Tata McGraw Hill, 2017
2. Robert L. Boylestad and Louis Nashelsky, Electronic Devices and Circuits Theory, Pearson/Prentice Hall, 11th Edition, 2015

Reference (s)

1. A.Salivahanan, N.Suresh Kumar, A.Vallavaraj, Electronic Devices and Circuits, Tata McGraw-Hill Publish-ing Company Limited, 2nd Edition, 2008
2. Visvesvara Rao, K. Bhaskara Rama Murty, K. Raja Rajeswari, P.Chalam Raju Pantulu, Electronic Devices and Circuits, Pearson Education, 2nd Edition, 2007
3. Millman and Grabel, Microelectronics, Tata McGraw Hill, 7thEdition, 2001
4. S.G.Burns and P.R.Bond, Principles of Electronic Circuits, Galgotia Publications, 2nd Edition, 1998

23EC302 Python Programming

3 0 2 4

Course Outcomes

At the end of the course, students will be able to

1. Illustrate the fundamentals of Python with syntax and semantics.
2. Use the concepts of conditional and control flow statements.
3. Demonstarte the concepts of strings, dictionaries, sets, list and tuples.
4. Demonstrate the concepts of Functions and Modules.
5. Use the concepts of files, searching and sorting mechanisms.
6. Demonstrate NumPy and Pandas.

COs – POs Mapping

COs	PO_1	PO_2	PO_4	PO_5	PSO_1
1	2		2	2	2
2	3	2	2	2	3
3	3	2	2	2	3
4	3	2	2	2	3
5	3	2	2	2	3
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction: Brief history and need for python programming, Running Python Scripts, Identifiers, Statements, Variables, Keywords, Input-Output statements, Indentation, command line arguments.
Data Types - Integers, Strings, Boolean **Operators**-Arithmetic, Comparison/Relational, Assignment, Logical, Bitwise, Membership, Identity
Expressions and order of evaluations- Precedence and Associativity.
Conditional Statements: Simple If, If-Else, Elif statement types, pass statements and iteration statements-While, For, Break, Continue
Applications of Python, REPL (Read, Evaluation, Print, Loop)
Practical Components

1. A) Write a Python program to perform the following operations on two integers a and b
   - Arithmetic operations
   - Logical operations

   B) Write a python Program to find the ASCII value of a Character and vice versa (use ord and chr methods).
   C) Write a python Program to convert a given decimal number into binary, octal and hexadecimal (use bin, oct and hex methods).
2. Write a Python program to check the given year is a leap year or not using if statement.
3. Write a Python program to use python generators to print all the prime numbers upto the given value n.
4. Write a Python program to check the given number is Armstrong or not using iteration statements.

12+8 Hours

Unit II

Introduction to Lists- List Traversals, Slicing, List Methods, List Comprehension and Multi-Dimensional List.
Introduction to Strings: String initialization and declaration, String Values, String Formatting and Multi Line Strings, String slicing.
Introduction to Tuple, Dictionary and Sets: Dictionary, dictionary operations and dictionary methods, Sets, set operations, Tuple, Tuple operations and methods
Methods Available in Python: eval syntax and its use cases, filter, reduce, map
Grouping with Dictionaries, Keyword Arguments
Practical Components

1. A) Write a Python program to flatten a nested list.
   B) Write a Python program to find the transpose of the matrix using list.
   C) Write a Python program to split a list into evenly sized chunks.
   D) Write a Python program in a given list of numbers create another list of even numbers using list comprehension.
2. A) Write a Python Program to remove punctuations from a String.
   B) Write a Python program to count the frequency of characters in the string and store them in a dictionary data structure.
3. A) Write a Python program in a given a list of n numbers, form a tuple of two numbers such that highest maximum and lowest minimum are in one tuple, second max and second min in other tuple and so on
   Eg: Given list of numbers 1, 4, 6, 2, 3, 5
   Output: ((6, 1),(5,2), (4,3))
   B) Write a Python program to find the cube of a given number using lambda()/anonymous function.
4. A) Write a Python program to find the squares of the list of numbers using map function.
   B) Write a Python program to print all the combinations for the given list of numbers using itertools.
   C) Write a Python program to print all the permutations for the given list of numbers using itertools.

12+8Hours

Unit III
Functions - Defining Functions, Calling Functions, Types of Arguments, Anonymous Functions, Scope of the Variables in a Function - Global and Local Variables.
Modules and Packages- Creating modules, import statement, from. Import statement, Math and itertools modules.
Files-Creating files, operations on files - Open, Close, Read and Write.
Searching and Sorting: Searching techniques-Linear search and Binary search. Sorting techniques-Bubble sort.
Insertion sorting, Applications of packages.
Practical Components

1. Define a function and write a method which accepts multiple parameters/ arguments and find the sum of given parameters.
2. Write a Python program to find the sum of the elements in the array using reduce function of the python.
3. Write a Python program to search a key element in the list using linear search approach.
4. Write a Python program to sort the given list using bubble-sort technique

12+8 Hours

Unit IV
NumPy & Pandas
NumPy- NumPy Library Introduction, Create NumPy array in python, functions in NumPy library, indexing, slicing and assigning NumPy array's, operations in NumPy Library.
Pandas- Pandas Library Introduction, series structures in Pandas Library, DataFrame structures in Pandas Library, element selection operations in DataFrame structures, structural operations on Pandas DataFrame, Multi indexed DataFrame structures, Structural concatenation operations in DataFrame, Functions that can be applied on DataFrame.
Sorting, mapping of DataFrame
Practical Components

1. A) Write a python program to Convert the given list to numpy array.
   B) Write a Python program to Remove rows in numpy array that contains non-numeric values.
   C) Write a Python program to Find the number of occurences of sequence in numpy array.
2. A) Write a python program to Combine one and two – dimensional numpy array.
   B) Write a Python program to Perform matrix multiplication on numpy arrays.
3. A) Write a Python program Create a pandas data frame with two dimensional list
   B) Write a Python program to Create a data frame from dict of numpy array.
4. A) Write a Python program to Clean the string data in the given pandas data frame.
   B) Write a Python program on Conditional operations on pandas data frame

12+8 Hours
Total: 48+32 Hours

Textbook (s)

1. Richard L. Halterman, "Fundamentals of Python Programming" , 3rd Edition, Southern Adventist University, 2019.
2. Willaim Mckenny, "Python for Data Analysis: Data Wrangling with Pandas, NumPy, and IPython" 2nd Edition, O'Reily 2017.

Reference(s)

1. Wesley J Chun, "Core Python Applications Programming", 3rd Edition, Pearson Education India, 2015.
2. Kenneth A. Lambert. "Fundamentals of Python: First Programs", 2nd Edition, Publisher: Cengage Learning 2018
3. Python Programming: A Modern Approach, VamsiKurama, Pearson 2017 Learning Python, Mark Lutz, Orielly, 5th Edition

23EC303 Logic Circuit Design

3 0 0 3

Course Outcomes

1. Illustrate the applications of Gates and Error Detection and Correction.
2. Identify a suitable tool (K-maps, Tabular etc.) to minimize Boolean expressions.
3. Implement combinational circuits using AOI and Universal logic gates.
4. Design combinational logic circuits using PLDs.
5. Analyse sequential logic circuits
6. Differentiate Mealy and Moore machines.

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_1
1	2				2
2	2				2
3	3	2			3
4	3	2	2	2	3
5	3	2	2	2	3
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I
Digital Logic Elements

Review of Basic Gates, EX-OR and EX-NoR gates, Universal Gates, realization of Gates using universal Gates, two level realization of logic functions using basic gates and universal Gates, Error Detection using parity bit, Error Detection and Correction using Hamming code. Applications of Gates.
Hexadecimal number system, Boolean rules

08 Hours

Unit II
Combinational Logic Circuits
Minterm, Maxterm, SOP, Standard SOP, POS, Standard POS, Minimization of logic functions using Karnaugh Map and Quine-McClusky method, Binary addition, Arithmetic Adders, Binary subtraction, subtraction using 1's complement and 2's complement methods, Arithmetic subtractors, Comparators, Ripple carry adder, carry look ahead adder, Encoder, Priority encoder, Decoder, Multiplexer, De-Multiplexer, Code converters,
GATES using MUX and Demultiplexers

16 Hours

Unit III
PLDs and Flip Flops
Programmable logic devices – PROM, PAL, PLA, Realization of Switching functions using PROM, PAL and PLA. Sequential logic circuits – RS latch using NAND and NOR Gates, Flip Flops – RS, J-K, T and D, Truth tables and Excitation Tables, Conversion of Flip Flops, Asynchronous Inputs.
Realisation of Flip Flops using MUX, CPLD

12 Hours

Unit IV
Sequential Logic Circuits
Registers - Buffer register, Controlled buffer register, Shift registers, Bi-directional shift register, Universal shift register, Asynchronous & Synchronous counters - Up, Down, Up down, Ring counters, Johnson counters, Mealy and Moore state machines – State assignment, state Diagram, state tables, Conversion of Mealy machine into Moore machine, Design of Mealy type serial adder and sequence detector, Minimization of completely specified state table using Partition table.
Sequence Generator, ASM Chart

12 Hours
Total: 48 Hours

Textbook (s)

1. A. Anand Kumar, Switching theory and logic design,PHI,3rd Edition 2016
2. Morris Mano, Digital Design,3rd Edition, PHI, 2001

Reference (s)

1. Zvi Kohavi, Switching & Finite Automata theory, 2nd Edition, TMH, 2008
2. R P Jain, Modern Digital Electronics, 3rd Edition, TMH, 2003

23EC305 Signals & Systems

3 0 2 4

Course Outcomes

1. Interpret various types of signals and systems and their operations
2. Explain signal approximation using Fourier series
3. Execute Fourier transform and Laplace transform of continuous signals
4. Summarise the characteristics of the LTI system and its properties
5. Compute LTI system response using convolution, correlation
6. Interpret sampling process and it's effects

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5	PSO_2
1	2			2	3	2
2	2			2	3	2
3	3	2		2	3	3
4	2		2	2	3	2
5	3	2	2	2	3	3
6	2		2	2	3	2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Introduction: Signal Analysis

Classification of Continuous time & Discrete time signals, Concept of impulse function, unit step function, Signum function, Signal operations, Power and Energy of signals, Orthogonal signal space, Signal approximation using orthogonal functions, Mean square error, Orthogonality in complex functions.

EEG, ECG signals

Practical Components

1. Familiarization with SCILAB/MATLAB: Matrix operations, plotting, relational operators, loops and functions
2. Generation of basic signals: Exponential, step, impulse, ramp, sinusoidal signals
3. Operations on signals: time reversal, time shifting
4. Operations on signals: amplitude scaling, time scaling

10+8 Hours

Unit II

Fourier Series and Fourier Transform

Representation of Fourier series for Continuous time periodic signals, Dirichlet's conditions, , properties of Fourier series, Exponential Fourier series, Relationship between Exponential Fourier series and trigonometric Fourier series, Concept of Fourier transform, Fourier transform of arbitrary signal, Fourier transform of standard signals, properties of Fourier transforms, Parseval's theorem, Hilbert Transform, Review of Laplace transforms, Inverse Laplace transform, Concept of region of convergence, Relation between Laplace & Fourier Transform.

Fourier series coefficients of Conjugate symmetry for real signals, Laplace transform of causal periodic signals

Practical Components

1. Find the trigonometric Fourier series coefficients of a rectangular periodic signal and reconstruct the Signal by combining the Fourier series coefficients with appropriate weights
2. Verification of Parseval's theorem
3. Find the Fourier transform of a square pulse. Plot its amplitude and phase spectrum
4. Draw the pole zero plot of given transfer function

14+8 Hours

Unit III

LTI Systems

Linear system, impulse response, Linear time invariant (LTI) system, Transfer function of a LTI system, Filter characteristics of linear systems, Distortionless transmission through a system, Ideal filter characteristics, Causality and Paley-Wiener criterion for physical realization.

Concept of convolution in time domain and frequency domain, Graphical representation of convolution, Cross

correlation and auto correlation of functions, properties of correlation functions, Energy density spectrum, Power density spectrum, Relation between convolution and correlation.
Detection of periodic signals in the presence of Noise by Correlation, Group delay

Practical Components

1. Design the first order low pass passive filter for given specifications and Plot the magnitude and phase response
2. Design the first order high pass passive filter for given specifications and Plot the magnitude and phase response
3. Generate the response of an LTI system for the given input and impulse response
4. Write a program to Check the given system is linear or not

13+8Hours

Unit IV

Sampling Theory

Sampling theorem: Graphical and analytical proof for Band Limited Signals, impulse sampling, Natural and Flat top Sampling, Reconstruction of signal from its samples, Aliasing, Bandpss sampling theorem
Zero-order Hold sampling, Interpolation

Practical Components

1. Find the Nyquist rate for a given signal.
2. Generate a discrete time sequence by sampling a continuous time signal.
3. Reconstruction of a signal from the discrete samples with aliasing effect.
4. Reconstruction of a signal from the discrete samples without aliasing effect.

11+8Hours

Total: 48+32 Hours

Text Book (s)

1. A.V. Oppenheim, A.S. Willsky and S.H. Nawab, Signals and Systems, PHI, 2nd Edition, 2015
2. Won Y Yang, Signals and Systems with MATLAB, Springer publications, 2014
3. B.P. Lathi, Signals, Systems & Communications, BS Publications, 2008

Reference Book(s)

1. Michel J. Robert, Fundamentals of Signals and Systems, MGH International Edition, 2nd Edition 2017
2. Simon Haykin and Van Veen,Wiley, Signals & Systems, PHI, 2nd Edition, 2007
3. C. L. Philips, J.M.Parr and Eve A.Riskin, Signals, Systems and Transforms, Pearson education, 3rd Edi-tion, 2004

23EC306 Electronic Devices and Circuits Lab

0 0 3 1.5

Course Outcomes

1. Demonstrate the operation of rectifiers
2. Assess the characteristics of special semiconductor devices
3. Implement the applications based on semiconductor devices
4. Show the characteristics of BJT and FET
5. Demonstrate the characteristics of amplifiers
6. Assess the frequency response of amplifiers

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_1
1	3	2		2	3
2	3	2		2	3
3	3	2		2	3
4	3	2	2	2	3
5	3	2	2	2	3
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

List of Experiments
Students will perform minimum fourteen Experiments

1. Half wave rectifier with and without filter.
2. Full wave center tapped rectifier with and without filter.
3. Bridge type Full wave rectifier
4. Design of Zener regulator.
5. Characteristics of SCR
6. Characteristics of UJT
7. Transistor CE input characteristic
8. Transistor CE output characteristic
9. Transistor CB input characteristic
10. Transistor CB output characteristic
11. Design of self-bias circuit
12. JFET characteristics
13. Characteristics of CE Amplifier
14. Characteristics of CS Amplifier
15. Frequency response of CE amplifier
16. Frequency response of CS amplifier

List of Augmented Experiments*

1. Design of Regulated DC Power Supply
2. Applications based on FET
3. Applications based on BJT
4. Applications based on SCR
5. Burglar Alarm

Reading Material (s)

1. N.N.Bhargava, D.C.kulshreshtha S.C.Gupta, Basic electronics and linear circuits Tata MC Graw Hill com-pany Ltd., New Delhi, 2nd Edition, 2003.
2. R.L. Boylestad and Louis Nashelsky, Electronic Devices and Circuits, Pearson/Prentice Hall, 9thEdition, 2006.

* Students shall opt any one of the Augmented experiment in addition to the regular experiments

23EC307 Logic Circuit Design Lab

0 0 3 1.5

Course Outcomes

1. Demonstrate the functionality of Combinational logic ICs
2. Design the Boolean functions logic using logic gates
3. Implement the combinational logic using logic gates
4. Implement the flip-flops using logic gate
5. Design the shift registers
6. Design the counters

COs –POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5	PSO_1
1	2			2		2
2	3	2		2		3
3	3	2		2	3	3
4	2		2	2	3	2
5	3	2	2	2	3	3
6	3	2	2	2	3	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

List of experiments

Students will perform minimum fourteen Experiments

1. Implementation of basic gates by using universal gates.
2. Realization of a Boolean function by using NAND-NAND and NOR-NOR logic.
3. Design a half adder circuit using gates and implement full adder using half adder
4. Design a half subtractor circuit using gates and implement full subtractor by using half subtractor
5. Implementation of BCD adder using 4bit binary adders
6. BCD to excess- 3 code converter.
7. Design of binary to gray code converter
8. Design a 4X1 multiplexer and 1X4 Demultiplexer using logic gates
9. Design a 8X3 Encoder and 3X8 Decoder using gates
10. Design a simple 2-bit multiplier using half adders
11. Design a BCD to 7-segment decoder/driver
12. Implementation of 8 bit binary comparator using 4 bit binary comparators
13. Implementation of D and JK flip-flops using NAND gates
14. Implementation of three bit SISO and three bit PIPO shift registers
15. Design of three bit synchronous up counter
16. Design of three bit asynchronous down counter

List of Augmented Experiments*

1. Design a Universal shift register.
2. Design a sequence detector
3. Design of ALU
4. Design a Digital Clock

Reading Material (s)

1. Morris Mano, Digital Design, PHI, 3rd Edition, 2001
2. Charles H. Roth, Fundamentals of Logic Design, Thomson Publications, 3rd Edition, 2014

* Students shall opt any one of the Augmented experiment in addition to the regular experiments

23ESX01 Employability Skills I

0 0 2 0

Course Outcomes

1. Demonstrate oral communication and writing skills as an individual to present ideas coherently
2. Develop life skills with behavioral etiquettes and personal grooming.
3. Assess analytical and aptitude skills.
4. Develop algorithms for engineering applications.
5. Solve engineering problems using software.
6. Utilize simulation tools for testing.

COs – POs Mapping

COs	PO1	PO2	PO3	PO5	PO8	PO10	PO12
1						3	2
2					1	2	2
3	2	1			2		
4	2		2	2			
5	2		2	2			
6	2		2	2			

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

1. Communication Skills, Confidence and Quantitative Aptitude

How Communication Skills affect Confidence? How to communicate effectively.(with Examples)

Listening: Listening?, Listening Vs Hearing, Possible reasons for why people do not Listen at times, Active Listening Vs Passive Listening, How Listening can affect our relationships? How Listening helps in Campus Placements also? (with Examples)

Goal Setting: SMART Technique to Goal Setting, Putting First things First, SWOT Analysis and Time Management

Attitude & Gratitude: Attitude Vs Skills Vs Knowledge, Attitude Vs Behaviour, How to develop Positive Attitude? Developing the attitude of Gratitude.

Public Speaking: JAM, J2M, Presentations by Students on General Topics.

7 Hours

2. Quantitative Aptitude

Number system, L.C.M and H.C.F, Problems on Ages, Averages, Time and work, Pipes and cisterns

8 Hours

Unit II

Verilog Language Constructs and Gate Level Modelling

Verilog as HDL, Levels of design description, Concurrency, Simulation and Synthesis, Functional verification, System tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis tools, Test benches, Keywords, Identifiers, White space characters, Comments, Numbers, Strings, Logic values, Strengths, Data types, Scalars and Vectors, Parameters, Memory, Operators, System tasks, AND gate primitive, Module structure, Other gate primitives, Tristate gates, Array of instances of primitives, Delays, Strengths and Contention Resolution, Net Types, Design of basic circuits. Design of Flip-flops with Gate Primitives, adders, Parameters, Path delays, Module parameters, Hierarchical access

Practical Components

1. Introduction to EDA tool and Simulation of logic gates
2. Design and Simulate Full adder and Full Subtractor
3. Simulate the Flip-Flops using the Gate Primitives

15 Hours

Total 30 Hours

23CSE01 Object Oriented Programming

3 0 0 3

Course Outcomes

1. Summarize object oriented programming concepts
2. Develop applications using different types of inheritances
3. Create simple applications using Interfaces, packages and collections
4. Analyse and recover runtime exceptions arise in the applications
5. Apply parallel processing applications using threads
6. Develop Interactive applications using AWT and Swing

COs–POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5
1	3	2			1
2	2	-			-
3	3	2	2		2
4	2	-		2	-
5	2	1		2	2
6	3	2	2	2	-

3–Strongly linked | 2–Moderately linked | 1–Weakly linked

Unit I

Introduction to Java

Features of object oriented programming, Overview of Object Oriented Programming principles, Importance of Java to the Internet, Byte code, Methods, classes and instances, Data types, arrays, control statements, simple java program, Classes and Objects– constructors, methods, access control, this keyword, overloading methods and constructors, garbage collection, String handling methods and String Tokenizer.

Java History–Computer Programming Hierarchy–Role of Java Programmer in Industry **11 Hours**

Unit II

Inheritance, Packages & Interface

Inheritance: Basics, Using super, Multilevel Hierarchy, Method overriding, Dynamic Method Dispatch, Using Abstract classes, Using final with Inheritance.

Packages: Defining, Creating and Accessing a Package, Understanding CLASSPATH, importing packages, Member access rules.

Interface: Defining an interface, differences between classes and interfaces, implementing interface, variables in interface and extending interfaces, Nested–Inner Class & Anonymous Classes.

Generic Class Types **13 Hours**

Unit III

Exception Handling & Multithreading

Exception handling: Concepts and benefits of exception handling, exception hierarchy, usage of try, catch, throw, throws and finally, built-in and User Defined Exceptions.

Multithreading: Definition thread, thread life cycle, creating threads, synchronizing threads, daemon threads, Inter Communication of Threads.

Control Flow in Exceptions **11 Hours**

Unit IV

Event Handling

The AWT class hierarchy, user interface components labels, button, Text components

Event Handling: Events, Delegation event model, handling mouse and keyboard events, Adapter classes, inner classes, compare basic AWT components with swing components, more user interface components-canvas, scrollbars, check box, choices, lists panels–scroll pane, dialogs, menu bar, layout managers, *java.util Package.*

Anonymous Inner classes a Short–cut to Event Handling **13 Hours**

Total: 48 Hours

Textbook (s)

1. H. Schildt, Java: The complete reference, 8th Edition, TMH, 2011
2. T. A. Budd, An Introduction to Object–Oriented Programming, 3rd Edition, Addison Wesley Longman, 2002

Reference (s)

1. Dietal & Dietal, Java: How to Program, 8th Edition, PHI, 2010
2. C. Horstmann, BIG JAVA Compatible with Java 5 & 6, 3rd Edition, Wiley Publishers, 2008
3. C. S. Horstmann and G. Cornell, Core Java, Vol 1. Fundamentals, 7th Edition, Pearson Education, 2004

23EC401 Analog and Digital Communications

3 0 0 3

Course Outcomes:

1. Explain Analog Modulation & Demodulation techniques
2. Summarise the noise level in Analog communication systems
3. Demonstrate the operations of Transmitters and Receivers
4. Explain different pulse modulation techniques
5. Illustrate different digital modulation and demodulation techniques
6. Illustrate different error control codes techniques

COs-POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_2
1	2				2
2	2				2
3	3	2	2		3
4	3	2		2	3
5	2			2	2
6	3	2	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Amplitude Modulation and Frequency Modulation

Introduction to communication system, need for modulation, Amplitude Modulation, power relations in AM waves, Generation and detection of AM waves: square law Modulator, envelope detector, Generation and detection of DSBSC Waves. SSB Modulated Wave, VSB modulation.
Frequency Modulation: FM Wave, Narrow band FM, Wide band FM, Generation and detection of FM Waves, Direct method of generation of FM waves, Balanced Frequency discriminator.
Switching modulator,-Frequency division multiplexing,

13 hours

Unit II

Noise, Analog Transmitters and Receivers

Noise in DSB & SSB System Noise in AM System, Noise in Angle Modulation System, Threshold effect in Angle Modulation System, Pre-emphasis & de-emphasis AM Transmitter, FM Transmitter - Variable reactance FM Transmitter, Super heterodyne receiver, Comparison of FM and AM Receiver.
Phase modulated FM transmitter, Phase locked loop

11 hours

Unit III

Pulse modulation

PAM, PWM, PPM, Model of Digital Communication Systems, Pulse Code Modulation: PCM Generation and Reconstruction, Quantization noise, Non uniform Quantization and Companding, Time Division Multiplexing, DPCM, DM and Adaptive DM.
Classification of line encoding techniques, TDM Frame Structures **12 hours**

Unit IV

Digital Modulations & Information theory

Digital Modulation Techniques: BASK, BFSK, BPSK, QPSK, generation and detection.
Baseband transmission: Base band signal receiver, probability of error and its analysis, the optimum receiver, matched filter.

Information Theory: Entropy, mutual information and Shannon's Channel Capacity Theorem, Fundamentals of error correction: Linear Block codes, cyclic codes, cyclic redundancy check *Telemetry, OQPSK*

12 hours
Total: 48 hours

Textbook (s)

1. H.Taub and D. Schilling, Principles of Communication Systems, TMH,4th Edition, 2017
2. Simon Haykin , Digital communications, John Wiley, 4th Edition,2013
3. Simon Haykin , An Introduction to Analog& Digital Communications, John Wiley, 2nd Edition, 2012
4. George Kennedy and Bernard Davis , Electronic Communication Systems, TMH, 4th Edition, 2004

Reference (s)

1. R.P. Singh, SP Sapre, Communication Systems TMH, 3rd Edition, 2017
2. B.P.Lathi, Zhi Ding, Modern Digital and Analog Communication Systems, Oxford, 4th Edition, 2011
3. John G. Proakis, Masond, Salehi, Fundamentals of Communication Systems, Pearson Education, 3rd Edition, 2008
4. H Taub & D. Schilling, Gautam Sahe, Principles of Communication Systems , TMH, 3rd Edition. 2007
5. Sam Shanmugam, Digital and Analog Communication Systems, John Wiley, 2005
6. Bernard Sklar, Digital communications Fundamentals and applications, 2nd Edition, PHI, 2001

23EC402 Analog Electronic Circuits

3 0 2 4

Course Outcomes

1. Outline the negative feedback amplifiers
2. Design Sinusoidal oscillators for a given frequency
3. Design power amplifiers and demonstrate the tuned amplifiers
4. Construct linear & nonlinear wave shaping circuits for given application
5. Design Multivibrator for a given frequency
6. Summarize different Time base circuits

COs –POs Mapping

COs	PO_1	PO_2	PO_4	PO_5	PSO_1
1	3	2	2	3	3
2	3	3	2	3	3
3	2				2
4	3	2	2	3	3
5	3	2	2	3	3
6	2				2

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

Feedback Amplifier & Sinusoidal Oscillators

Feed Back amplifiers - Concept of feedback, Effect of negative feedback on the amplifier characteristics, Topologies, Voltage Series, Current Series, Voltage Shunt and Current Shunt feedback Amplifiers.

Oscillators- Condition for oscillations, Hartley oscillator, Colpitts oscillator, RC phase shift oscillator, Wein bridge Oscillator, Crystal Oscillator.

Clapp oscillator, Tuned collector oscillator, Stability of oscillators

Practical Components

1. Design and simulate current series feedback amplifier and observe its frequency response.
2. Design and simulate Hartley oscillator for given frequency and observe the desired output waveforms.
3. Design and simulate RC phase shift oscillator for given frequency and observe the desired output waveforms.
4. Design and simulate the Wein bridge oscillator for a given frequency and observe the desired output waveforms.

13+ 8 Hours

Unit II

Power Amplifiers & Tuned Amplifiers

Class A power amplifier, Efficiency of Class A power amplifier - Resistive load, Transformer load, Class B power amplifier- Efficiency of Class B power amplifier- Push Pull, Complimentary Symmetry, Class C power amplifier, Class D power amplifier.

Single Tuned Capacitive Coupled Amplifier - Quality factor of a tank circuit, Gain & Bandwidth, Stagger tuned amplifiers,

Application of Tuned Amplifiers, Neutralization techniques

Practical Components

1. Simulate a Class A resistive load amplifier and find the efficiency.
2. Simulate a Class A transformer load amplifier and find the efficiency.
3. Observe the frequency response of a single-tuned amplifier.
4. Observe the frequency response of a stagger-tuned amplifier.

12+ 8 Hours

Unit III

Linear & Non Linear Wave Shaping Circuits

Response of High pass & Low pass RC circuits with sinusoidal, step, pulse, square inputs. RC network as differentiator and integrator, Attenuators.

Diode clippers, Transfer characteristics of clippers, Comparators, Clamping operation, clamping circuits using diode with different inputs, Clamping circuit theorem.

Double differentiator, Applications of voltage comparators

Practical Components

1. Design and simulate a high-pass RC circuit for square wave input and observe the response.
2. Design and simulate a low-pass RC circuit for square wave input and observe the response.
3. Design and simulate different types of clipping circuits for given sinusoidal input and observe the desired output waveforms.
4. Design and simulate different types of clamping circuits for a given input and observe the desired output waveforms.

12+8 Hours

Unit IV

Non Sinusoidal Waveform Generators

Collector coupled Astable Multivibrator, Monostable Multivibrator, Bistable Multivibrator, Schmitt Trigger. General features of a time base signal, Voltage sweep generators using UJT, Miller and Bootstrap time base generators, Current time base generators.

Application of Multivibrator, Applications of Time base generators

Practical Components

1 Simulate the Astable multivibrator and observe the desired waveforms at each base and Collector.
2 Simulate the Monostable multivibrator and observe the desired waveforms at each base and Collector.
3 Simulate the Bistable multivibrator and observe the desired waveforms at each base and Collector.
4 Design and simulate UJT Relaxation Oscillator to generate time base signal.

11+8 Hours

Total : 48+32 Hrs

Textbook (s)

1. J.Millman, C.C.Halkias and Chetan D Parikh, Integrated Electronics, 2ndEdition, Tata McGraw Hill, 2017
2. A. Anand Kumar, Pulse and Digital Circuits, PHI, 2005

Reference (s)

1. K.Venkata Rao, K.Rama Sudha, Electronic Devices and Circuits, McGraw Hill, 1st Edition, 2015
2. VenkataRao.K, RamaSudha.K and Manmadha Rao.G, Pulse and Digital Circuits, Pearson Education, 1st Edition, 2012
3. Robert L. Boylestad and Louis Nashelsky, Electronic Devices and Circuits Theory, Pearson/Prentice, 11th Edition, 2012
4. J. Millman, H. Taub and M. Surya Prakash Rao, Millman's Pulse, Digital and Switching Waveforms, McGraw-Hill, 3rd Edition, 2010
3. M.H. Rashid, Thomson, Micro Electronic Circuits: Analysis and Design, PWS Publishers,1999

23EC403 Electromagnetic Waves & Transmission Lines

3 0 0 3

Course Outcomes:

1. Demonstrate the laws & theorems of static electric and magnetic fields.
2. Demonstrate the behaviour of time-varying electromagnetic fields using Maxwell's equations.
3. Outline the electromagnetic wave propagation in different media.
4. Demonstrate the characteristics of EM waves.
5. Illustrate the parameters of transmission lines.
6. Outline the impedance transformation techniques.

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PSO_2
1	2				2
2	2				2
3	3	2	2		3
4	2			2	2
5	3	2	2	2	2
6	3	3	2	2	3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

UNIT I

Static Electric and Magnetic Fields: Review of Co-ordinate Systems, Coulomb's Law, Electric Field Intensity, Electric Flux Density, Gauss Law and Applications, Electric Potential, Energy Density, Illustrative Problems, Biot-Savart Law, Ampere's Circuital Law and Applications, Magnetic Flux Density, Magnetic Scalar and Vector Potentials, Forces due to Magnetic Fields, Illustrative Problems. **12 Hours**

Capacitance of parallel plate, coaxial and spherical capacitors, Inductance of solenoid and toroid

UNIT II

Maxwell's Equations : Faraday's Law and Transformer EMF, Inconsistency of Ampere's Law and Displacement Current Density, Maxwell's Equations in differential & integral forms along with word Statements, Conditions at a Boundary Surface, Illustrative Problems, Wave Equations for Conducting and Perfect Dielectric Media, Uniform Plane Waves – Definition, Relation between E & H components, Wave Propagation in perfect dielectrics, free space, good dielectrics, good conductors, skin depth, Illustrative Problems. **12 Hours**

Surface Impedance, Power Loss in a Plane Conductor

UNIT III

EM Wave Characteristics: Polarization & Types, Reflection and Refraction of Plane Waves – Normal and Oblique Incidences for both Perfect Dielectric and Perfect Conductor, Brewster Angle, Critical Angle and Total Internal Reflection, Poynting Vector and Poynting Theorem, Illustrative Problems. **10 Hours**

Time harmonic fields, Complex Poynting vector

UNIT IV

Transmission Lines: Types, Equivalent Circuits, Transmission Line Equations, Primary & Secondary Constants, Expressions for Characteristic Impedance, Propagation Constant, Phase and Group Velocities, Infinite Line, Lossless lines, distortion less lines, Illustrative Problems, Input Impedance Relations, Reflection Coefficient, VSWR, Average Power, Open & Short Circuited Lines, and Matched Lines, Low loss radio frequency and UHF Transmission lines, UHF Lines as Circuit Elements, Smith Chart – Construction and Applications, Quarter wave transformer, Illustrative Problems.

14 Hours

Single Stub Matching, Double Stub Matching

Textbook (s)

1. Matthew N.O. Sadiku, Elements of Electromagnetics, Oxford University Press, 7th Edition, 2020.
2. Transmission Lines and Networks, Umesh Sinha, 8th Edition, Satya Prakashan Tech. India Publications, New Delhi, 2003.

3. Gottapu Sasibhushana Rao, Electromagnetic Field Theory and Transmission Lines, Wiley Publishers, 1st Edition, 2012.
4. John A. Buck, William H. Hayt, Engineering Electromagnetics, Tata McGraw Hill, 8th Edition, 2011.

Reference (s)

1. Electromagnetic Waves and Radiating Systems, E.C. Jordan and K.G. Balmain, 2nd Edition, PHI, 2000.
2. Joseph Edminister, Electromagnetics, Schaum Outline Series, McGraw Hill, 2nd Edition, 2007.
3. Networks, Lines, and Fields, John D. Ryder,2nd Edition, PHI publications, 2012.
4. G.S.N. Raju, Electromagnetic Field Theory and Transmission Lines, Pearson Education, 1st Edition, 2006.

23CSE02 Object Oriented Programming Lab

0 0 3 1.5

Course Outcomes

1. Make use of JAVA SDK environment to create - debug and run java programs
2. Create applications based on code reusability
3. Develop programs using threads
4. Develop and debug real time problems using exception handling
5. Using IDE, create interactive applications using event handling mechanisms
6. Design Graphical User Interface using AWT components and Swing

COs – POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5
1	1	3		3	1
2	2	3		3	1
3	3	2		2	1
4	2	2	2	3	1
5	3	2	2	3	2
6	3	2	2	2	2

3 – Strongly linked | 2 – Moderately linked | 1 – Weakly linked

List of Experiments

Students will perform minimum twelve Experiments

Write Java programs to:

1. Demonstrate the basics of Java using classes, methods and objects.
2. Develop a java program that print all real solutions to the quadratic equation ax2+bx+c=0
3. Demonstrate String handling methods.
4. Demonstrate this keyword in different ways
5. Demonstrate the different types of inheritance concept.
6. Demonstrate Inheritance concept using method overriding, super & final keywords and runtime polymorphism
7. Create a java Program to achieve multiple inheritance
8. Implement matrix operations using multidimensional arrays
9. Create a package which has classes and methods to read Student Admission details
10. Extracting tokens using StringTokenizer
11. Handle checked and unchecked exceptions using try-catch, finally, throw and throws keywords
12. Handle user-defined Exceptions
13. Develop a java program for thread Synchronization using by synchronized method and block.
14. Design a Job Application/ Student Admission Form and store the values in a file
15. Handle simple event to display cut/copy/paste events using Swings
16. Emulate the working of a simple Calculator.

List of Augmented Experiments

1. New Patient Registry Management System
2. Restaurant Billing Management System
3. Library Management System
4. ATM Management System
5. Bus Ticket Booking Management System
6. Movie Ticket Booking Management System
7. Queuing Management System
8. Attendance Management System
9. Medical Store Billing Management System
10. Text Editor Projects in Java
11. Google Search Engine Filter
12. Electronic voting System
13. Day Planner
14. Library management System
15. Personal Finance Management System

Reading Material (s)

1. JAVA Lab manual, Department of CSE and IT, GMR

* Students shall opt any one of the Augmented experiment in addition to the regular experiments

23EC405 Analog and Digital Communications Lab

0 0 3 1.5

Course Outcomes

1. Assess the sampling theorem
2. Demonstrate modulation techniques
3. Demonstrate demodulation techniques
4. Implement different Baseband modulation techniques
5. Demonstrate different Digital modulation techniques
6. Contrast the design issues in a digital communication system

COs-POs Mapping

COs	PO_1	PO_2	PO_3	PO_4	PO_5	PSO_2
1	3	2		2		3
2	3	2		2	3	3
3	3	2		2	3	3
4	3	2	2	2		3
5	3	2	2	2		3
6	3	3	2			3

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

List of Experiments

Students will perform minimum twelve Experiments

1. Verification of Sampling Theorem
2. Amplitude Modulation & Demodulation
3. AM-DSB SC -Modulation & Demodulation
4. Design of envelope Detector
5. Frequency Modulation &Demodulation
6. Pulse Amplitude Modulation–Modulation& Demodulation
7. PWM, PPM -Modulation & Demodulation
8. Pre-emphasis & de-emphasis
9. Phase Locked loop(PLL)
10. Verify the operation of Time Division Multiplexing
11. Verification of Delta Modulator
12. Generation and Detection of pulse code modulation
13. Generation and Detection of Differential Pulse Code Modulation
14. Generation and Detection of ASK
15. Generation and Detection of PSK
16. Generation and Detection of of FSK

List of Augumented Experiments*

1. Design of AM receiver
2. Mobile Phone Detector
3. FM Transmitter
4. FM Receiver
5. HAM Radio Receiver

Reading Material(s)

1. Simon Haykin , Digital communications, John Wiley, 4th Edition, 2013
2. H.Taub and D. Schilling, Principles of Communication Systems, TMH, 4th Edition, 2017
3.John G. proakis, Masoundsalehi, Gerhard bakh ,Contempary communication system using MATLAB &Simulink,Thomson India publishers, 2007

* Students shall opt any one of the Augmented experiment in addition to the regular experiments

23ESX01 Employability Skills I

0 0 2 2

Course Outcomes

1. Demonstrate oral communication and writing skills as an individual to present ideas coherently
2. Develop life skills with behavioral etiquettes and personal grooming.
3. Assess analytical and aptitude skills.
4. Develop algorithms for engineering applications.
5. Solve engineering problems using software.
6. Utilize simulation tools for testing.

COs – POs Mapping

COs	PO1	PO2	PO3	PO5	PO8	PO10	PO12
1						3	2
2					1	2	2
3	2	1			2		
4	2		2	2			
5	2		2	2			
6	2		2	2			

3–Strongly linked | 2–Moderately linked| 1–Weakly linked

Unit I

1. Building Confidence

Fear? Steps to Overcoming the Fear of Public Speaking?
Self Esteem: Definition? Types of Self Esteem, Causes of Low Self Esteem, Merits of Positive Self Esteem and Steps to build a positive Self Esteem.
Group Discussions (Practice): GD? GD Vs Debate, Overview of a GD , Skills assessed in a GD, Dos & Don'ts, & Conducting practice sessions (Simple Topics).
Motivational Talk: Team Work: Team Vs Group? Stages in Team Building, Mistakes to avoid and Lessons to Learn (Through Stories or Can be a Case Specific)

8 Hours

2. Quantitative Aptitude

Percentages, Profit and loss, Mixtures and Allegations, Simple Interest, Compound Interest

7 Hours

Unit II

Behavioural Level Modelling

Operations and Assignments, Functional Bifurcation, Procedural constructs: Initial, Always, Assignments with delays, Wait, Multiple always blocks Designs at Behavioural level, Blocking and Non-blocking assignments, Case statement, Simulation flow, Conditional statements, and loops- if, if-else, repeat, for, while, forever, parallel blocks, force-release, Event, System Tasks, and Functions, File based tasks and Functions, Compiler directives, User-Defined Functions, Tasks and Primitives-Introduction, Function, Tasks, User- Defined Primitives (UDP)
Continuous assignment structures, Delays, and Continuous assignments, Assignment to Vectors, Operators,

Practical Components

1. Perform Behavioural model for multiplexer and demultiplexer
2. Perform Behavioural model for 8 to 3 priority encoders
3. Perform Behavioural model for 4-bit counter and shift register
4. Perform the simulation of parity bit generation using functions and tasks
5. Performa two-bit binary addition using functions and tasks
6. Perform the simulation of half adder and display the stimulus, response of system tasks- $monitor,$display,$monitoron, $monitorof, $stop, $finish

15 Hours
Total 30 Hours